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DISPLAY SYSTEM FOR SELECTIVELY OVERLAYING SYMBOLS AND GRAPHICS ONTO A VIDEO SIGNAL

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(71) Applicant *(for all designated States except US)*: SCIENTIFIC-ATLANTA, INC. [US/US]; One Technology Parkway, South, Norcross, GA 30092 (US).

(71)(72) Applicants and Inventors: BANKER, Robert, O. [US/US]; 1581 Chamblee Gap Road, Cumming, GA 30130 (US). ITH, Cham [US/US]; 3749 Roanoke Court, Duluth, GA 30136 (US). BACON, Kinney, C. [US/US]; 2820 Springtime Court, Lawrenceville, GA 30243 (US). BURLESON, David, B. [US/US]; 110 Glenclairn Court, Roswell, GA 30076 (US).

(74) Agents: POTENZA, Joseph, M. et al.; Banner, Birch, McKie & Beckett, Suite 1100, 1001 G Street, N.W., Washington, DC 20001-4597 (US).

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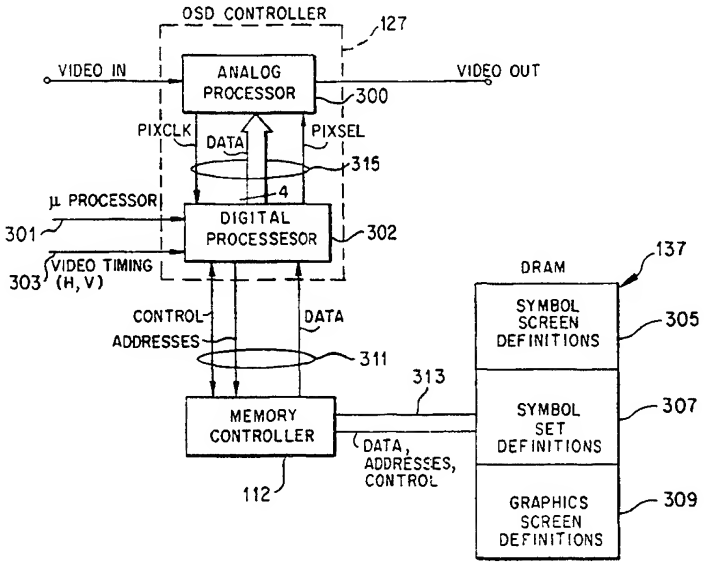

(57) Abstract

An on screen display system for a subscription television system includes a display processor (127) which can be preprogrammed by the control processor (128) with a plurality of display attributes including different symbol sets, color palettes, whether the screen is to comprise text, graphics, or a combination thereof, and the size and location of each screen display area. The display processor (127) includes a digital processor (302) which controls accessing of the display data from the memory and converting the data to timed digital pixels and an analog processor (300) with digital-to-analog converter (314), which produces analog pixels from the digital pixels in a timed relation to an input video signal, and multiplexer (316), which substitutes the analog pixels for the pixels of the input video signal when the display processor is active.

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DISPLAY SYSTEM FOR A SUBSCRIBER TERMINAL

Field of the Invention

The invention pertains generally to a subscriber terminal for CATV or other subscription television systems and is more particularly directed to an on-screen display system for such subscriber terminals.

Background of the Invention

The subscriber terminal, more commonly known as a set top terminal, is an integral component of subscription television systems. These subscription television systems can be cable television (CATV) systems, multi-point, multidistribution subscription (MMDS) systems, or direct-to-home (DTH) systems. The terminals have conventionally provided the functions of tuning particular channels of the subscription system which are outside the subscriber's television receiver capability. Further, they provide conditional access to the particular subscription service through authorization codes and in many services provide tiering or authorization of particular channels of the service by descrambling.

More recently, the subscriber terminal has become user friendly by providing an interactive, on-screen display and other user functions that allow the subscriber to manipulate the cable service and his television receiver in additional ways. These features include such things as volume control, pay-per-view event confirmation, favorite channel listings, sleep timer features, parental control capability, program timers for recording VCR programs and other types of consumer friendly operational features.

In addition, some of the features found in newer television receivers can be provided for older receivers by the subscription terminal. For example, channel identity, mute and volume control functions can be accomplished by the subscriber terminal making the subscriber's television receiver appear to be a newer model with these capabilities.

An advantageous example of a subscriber terminal with these advanced consumer features is the Model 8600 series of subscriber terminals manufactured by Scientific-Atlanta, Inc. of Norcross, Georgia.

These terminals generally provide on-screen displays by combining the video signal from a selected channel with an on-screen display video signal from a video generator prior to the remodulation of the combination to either Channels 3 or 4. The subscriber terminal generates timed control codes to the video generator which describe the various displays which are to be provided on the subscriber's television screen.

However, with the totality of the new features which are available in the advanced subscriber terminals, the flexibility and memory capability of the terminal for onscreen display has been exceeded. This is particularly the case in the area of providing specially defined characters or specially sized characters. Conventional video generator chips usually provide a limited set of characters and a single or severely restricted set of character fonts. For a truly flexible system, a bit-mapped or full graphics mode should be used. This type of graphic system however has been too memory and computationally intensive for subscriber terminals in the past. Further, there is generally no method for reprogramming a subscriber terminal to change the graphics capability of a display once it has been delivered to a subscriber. This makes the user interface extremely difficult to update or upgrade.

What is needed is an advanced display system which is flexible and powerful enough to support the advanced features available today in subscriber terminals and which will be capable of supporting the features which will be incorporated into the subscriber terminals of the future.

Summary of the Invention

An improved on screen display system for a subscriber terminal is provided by the invention. The display system compromises a display processor and a display memory which is

partitioned into a symbol screen definition section, a symbol set definition section, and a graphics screen definition section. The symbol screen definition section is programmable with a plurality of symbol pointers which select particular symbols from one or more of the symbol set definitions and the sequence of displaying those symbols. The graphics screen definition section of the memory is programmable with a pixel display of the entire screen. The display system is extremely flexible in that its many features allow on screen displays to be generated easily, manipulated easily, and displayed quickly with an optimal use of the memory and control processor resources of the subscriber terminal.

The display processor is utilized to process the display information from the display memory and convert the display data into an on screen display for the subscriber terminal. The display processor can produce a text or symbol display, a graphics display, or combinations of text and graphic displays. One feature of the system permits either a symbol display, graphics display, or a combination of both to be displayed on the display area. This flexibility permits pure symbols (all text) to be written, or text with an overlay of graphics, such as a logo or the like. Another feature allows each of the different types of displays to be of different sizes and positioned at various locations of the display area.

The display processor processes the display information into an on screen display in conjunction with a plurality of display attributes or parameters. The display parameters include information concerning the height and width of a defined set of symbols. The symbol definitions and the display parameters are programmable into the subscriber terminal memory which means there can be a multiplicity of symbol definitions sets to choose from, and each symbol set can be of a different size. The flexibility of allowing more than one symbol set to be defined and the ability to manage its size, allows the facile display of non-English character sets such as Chinese, Japanese, Arabic, etc. Thus, the symbol displays have an important use in generating text displays in various languages and character

fonts. The symbols are provided as different sizes of arrays of pixels which can be formed into symbol sets, for example, to define an English language character set of a particular size and style.

In one preferred embodiment, the symbols can be arranged horizontally on the display in a plurality of symbol lines which can then be given line attributes. In this manner, single lines of text can be given a common denominator which can be changed by changing the line attribute without having to reprogram every character in a line. The line attributes which the invention provides, as by way of illustrative example, include variation of the symbol set definitions, the color of an underline for a character, and a palette selection for that underline color. By providing a method of varying the symbol sets for the symbol lines, each symbol line can be not only a different size or font of character, but even a different language. These several choices of line attributes can be displayed simultaneously on the same on-screen display. It is evident that many other line attributes could be provided in this manner.

Each symbol of a symbol set definition is defined as an array of pixels, mxn, which is stored in display memory as one or more bits corresponding to each pixel. In the preferred embodiment, the number bits of each pixel corresponds to a number of pixel attributes which can be represented by the separate states of that number of bits. For example, for a single bit per pixel, two states (two attributes) can be stored for each pixel. In the illustrated implementation, two bits per pixel are used to define the color attributes of the pixel for a symbol or character. The four states of the two bits allow the selection of either a foreground color, a background color, the color black, or the color white for each pixel. These choices produce a great flexibility in choosing a style or character font for a symbol in a minimum amount of memory which can then be easily colored in a multiplicity of hues and tints.

The symbol screen definition section of the display memory is programmed with pointers to the particular symbols which are to make up the display. The pointers address each symbol in one

of the symbol set definitions. Additionally, in the illustrated implementation, the pointers also describe symbol attributes which are easier to describe for the individual symbols or for which changes may be desired without changing the symbol style (symbol definition). In the illustrated implementation the pointer contains a representation of the color of the symbol, a foreground mode bit, whether it should be underlined, and whether it should blink.

This produces a system where each pixel in each symbol can be one of four colors, either a black, white, or background color or a foreground color. Because the pointer of a symbol selects the pair of palette registers, it will choose the foreground and background colors for the symbol for example, a blue letter on a white background. To change such a color combination, a programmer selects a different color combination with the address of a different pair of palette registers. In the present display system, up to sixteen different color combinations can be stored for selection at any one time.

The pointer to the symbol definition also contains the foreground mode bit which allows for the effortless selection between white and black characters on multiple color backgrounds. If this bit is in one state, then colors are displayed normally. Alternatively, if this bit is in its other state, the effect of the colors of black and white are reversed for the foreground palette registers. If the entire foreground palette registers are with the color white and the background palette registers are loaded with sixteen distinct colors, then either black or white characters can be displayed on sixteen different colored backgrounds. Only the foreground mode bit in the symbol pointer needs to be changed to select between white and black characters while the same symbol definition can be used.

The foreground mode bit works by inverting the luminance value of the particular palette register selected. Therefore, it further provides an effect for colored symbols. Setting this bit causes the intensity of colored symbol to be reversed such

that bright characters will become dim and dim characters will become bright.

The display processor also provides a feature for displaying the symbols on a background of active video. Normally, the symbols have a foreground color for the symbol pixels of the symbol array and a background color for the background pixels of the symbol array. The symbol array pixels are then substituted for the pixels of active video and the foreground colors and background colors fill the screen, i.e., white letters on a blue background. However, the active video background feature inverts the choice of the symbol array pixel versus the active video pixel making the background pixels of the symbols appear transparent.

A unique method of making this selection is by assigning a particular color or group of colors to a pixel to be a transparent color. When that color is sensed, the display system, instead of attempting to convert that pixel into a color, selects the active video pixel for substitution. In a preferred implementation, the choice of the color to be a transparent pixel is an out of range color, for example, one where the luminance equals zero for nonzero chroma components R-Y or B-Y.

The graphic screens, which are pixel mapped arrays, may additionally use this feature. Because each pixel of a graphics screen has a defined color, that color can be selected as a transparent color which will cause the selection of the active video pixel. In this manner, the graphics screens can be easily overlayed on active video to show cutout portions of the active video and other special effects.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and aspects of the invention will be more clearly understood and better described if the following detailed description of the preferred embodiments is read in conjunction with the appended drawings wherein:

Fig. 1 is a system block diagram of a subscription television system of the CATV type which includes a multiplicity of subscriber terminals;

Fig. 2 is a detailed block diagram of one of the subscriber terminals of the system illustrated in Fig. 1;

Figs. 3-7 are a pictorial representation of the different modes of the on screen display system of the subscriber terminal illustrated in Fig. 2;

Fig. 8 is a pictorial representation of a pointer of the symbol screen definition section of the display memory;

Fig. 9 is a pictorial representation of a generic symbol of the symbol set definition area of the display memory;

Fig. 10 is a pictorial representation of the palette registers used in the color selection for symbol;

Fig. 11 is a functional block diagram of the display controller illustrated in Fig. 2 and a pictorial representation of the display memory partitioned into a symbol screen definitions section, a symbol set definitions section, and a graphics screen definitions section.

Fig. 12 is a detailed block diagram of the analog processor illustrated in Fig. 11;

Fig. 13 is a detailed block diagram of the processor illustrated in Fig. 11;

Fig. 14 is a pictorial representation of the mapping of the configuration registers for the digital processor illustrated in Fig. 13;

Figs. 15-20 are detailed electrical schematic diagrams of the various parts of the digital processor illustrated in Fig. 13;

Fig. 21 is a detailed electrical schematic diagram of the various parts of the analog processor illustrated in Fig. 12;

Fig. 22 is a functional flow chart illustrating the data flow for displaying symbols with the system illustrated in Fig. 11; and

Fig. 23 is a functional flow chart illustrating the data flow for displaying graphics with the system illustrated in Fig. 11.

Detailed Description of the Preferred Embodiments

A subscription television system of the CATV type is more fully illustrated in Fig. 1. The subscription television system includes a headend 10 and a plurality of subscriber terminals 40, 44 and 48 which are connected over a distribution system 52. As is conventional, the distribution system 52 may include coaxial or optical fiber cable, system amplifiers, line extenders, etc. The headend 10 is under the supervision of a system manager 12 which controls a hardware controller, headend controller 22. A billing computer 11 communicates with the system manager 12 to authorize and transmit transactions to subscribers.

The television or other programming for the subscription system may come from a satellite downlink where it is decoded and demodulated by satellite receivers 18 into a number of channels. Each channel is either applied to a modulator 24 and 30 or a scrambler and modulator 26 and 28 which, under the control of the headend controller 22, remodulates the channels to the frequencies of the local subscription system channel line up. For a premium or restricted channel service (tiered, pay-perview, or the like), some channels are scrambled by any of the known CATV methods by the scramblers and modulators 26 and 28. While the other channels can be transmitted without conversion. The program channels are then frequency division multiplexed onto the distribution system 52 by an RF combiner 34 as a broadband television signal. The plurality of channels of programming can then be transmitted over the distribution system 52 and supplied to each of the subscriber terminals 40, 44, and 48.

The scramblers and modulators 26 and 28 further may include the function of data insertion for its particular channel. This method of providing the data within the channel signal is generally termed in-band signaling. The data may be applied to any audio portion, video portion or both the audio and video portions in combination, or any other portion of the television channel. Many subscription television systems have amplitude

modulated data pulses on the audio subcarrier. Further, in other subscription television systems, data may be inserted into the vertical and/or horizontal blanking intervals of the video portion.

The data which is inserted into the television channel in this manner can be conditional access data to globally or locally address and control the subscriber terminals 40, 44 and 48, on screen text data, or other types of information from the headend controller 22. Other data and information, such as electronic program guides and information services, can be inserted into the channels from a data controller 20. The data controller 20 can receive local data or national data from the satellite downlink through the satellite receiver 18.

In addition, data can be transmitted over the distribution system 52 by out-of-band signaling. In this mode, the system manager 12 accesses an addressable transmitter 32 with transactions to transmit this data. The addressable transmitter 32 may be used to modulate a data signal on a frequency not associated with the television programming. The broadband television programming of the cable systems has generally been applied from 50 Mhz to 550 Mhz and above, while out-of-band signaling systems have been used in non-video portions of these signals, such as at 108.2 Mhz with a frequency shift keying modulation technique. These transactions are combined with the broadband television signal at 36 and transmitted to the subscriber terminals 40, 44 and 48.

Transactions in the system are designated as addressed (to a particular subscriber terminal or group of subscriber terminals) or global (to all subscriber terminals). These transactions are in a standardized format which can be sent over any of the communication paths mentioned.

Signaling and data information may also flow in the reverse direction from the subscriber terminals to the headend via a reverse signaling path through the distribution system 52. In one form, the reverse signals are digital biphase shift keying (BPSK) modulated and applied to a frequency below 50 Mhz. The signals flow back from the subscriber terminals to an IPPV

processor where they are decoded. In addition, any of the subscriber terminals 40, 44 and 48 may include a modem and telephone link 52 to a telephone processor 16 at the headend 10. The information from processors 14 and 16 are directed to the system manager 12, which communicates to the billing computer 11 to obtain authorization and billing information. The reverse signaling system has generally been used for ordering pay-per-view (PPV) or impulse-pay-per-view (IPPV) events. In the future the reverse signal path may be used for any number of additional interactive services.

Referring to Fig. 2, a detailed block diagram of one of the subscriber terminals, for example, the one indicated as 40 of the subscription television system will now be described. The broadband television signal from signal distribution system 52 is received at the input of up/down converter or tuner 100. An out-of-band data receiver 150 is also coupled to the broadband input. Conventionally, the up/down converter 100 may include an input filter, such as a diplexer, to separate the 108.2 Mhz out-of-band signal and the broadband television signal. The up/down converter 100 can be tuned to a predetermined channel for receiving in-band video and audio data when not in use. The channel may be predetermined from the system manager 12 and, by one of the data transmission methods described herein, the predetermined channel identification can be stored in subscriber terminal 40.

When in use, the up/down converter 100 is tuned according to a channel entered by a subscriber via a user interface having an IR receiver 124, remote control 126 and terminal keypad 122. Up/down converter 100 uses a phase locked loop under the control of a tuning control 102 to convert the selected or predetermined default RF channel signal to a 45.75 Mhz intermediate frequency signal. A multifunction control circuit (MCC) 104, preferably an application specific integrated circuit (ASIC) combining many subscriber terminal control and data handling functions into a single package, is linked to up/down converter 100 by a bidirectional link to the tuner control 102. The link has one path for tuning and a return link for feedback control of the

tuning process. A feedback signal for automatic gain control and one for automatic frequency control are transmitted to the up/down converter 100 through filters 101, 103, respectively from a video demodulator 109.

A filter, such as a SAW filter 106, filters the IF channel signal to split the signal into separate video and audio portions for further processing. The video portion is demodulated and descrambled by the video demodulator 109 under the control of a descrambler control 110 of the MCC 104. The video demodulator 109 performs the sync restoration (descrambling of the video signal) for sync suppression scrambling. The video signal then passes through a band pass filter 130 and to a video inverter 132 where inverse video inversion (descrambling) takes place. The descrambling of the video portion, whether sync suppression, sync inversion, video line inversion, etc. is under the control of the descrambler control 110 of the MCC 104. The descrambler control 109 provides the necessary timing signals, inversion axis levels, and whether the video is inverted or not to the video inverter 132 and supplies the necessary timing, restoration levels and identification of sync pulses to be restored to the demodulator 109. The descrambler control 110 usually receives such descrambling information from pulses as in-band audio data.

In the other path, the audio signal is converted from the 41.25 Mhz IF carrier to the intermodulation frequency of 4.5 Mhz by a synchronous detector 105. Feedback for automatic gain control of detector 105 is supplied from the output of band pass filter 131. The audio signal may then be demodulated by an FM demodulator 119. An amplitude modulation detector 111 performs pulse detection to recover the in-band audio data which are amplitude modulated onto the audio carrier. The recovered in-band pulses are supplied to an in-band audio data decoder 117 of MCC 104 for processing after being shaped by pulse shaper 115. The in-band data, except for descrambling data, is stored in DRAM 137 for buffering. Descrambler control 104 accesses descrambling data directly for the video descrambling operation.

Volume control of the audio signal is performed under the

control of a volume control 118 of the MCC 104 and the microprocessor 128 as described in U.S. Patent No. 5,054,071, incorporated herein by reference. After volume control, the audio signal is passed through a low pass filter 123 and a mute switch 125. The output of the mute switch 125 is applied to a modulator 142.

The MCC 104 receives the video signal after demodulation and descrambling and detects the in-band video data from the VBI of the signal with a VBI decoder 129. The in-band video data is transmitted at a frequency on the order of known teletext systems, such as about 4.0 megabits per second, and a data clock provides an appropriate sampling frequency higher than the Nyquist rate according to well known techniques. The in-band decoder 129 stores the data in DRAM 137 prior to processing by the microprocessor 128, the DRAM 128 serving as a data buffer.

The output of video inversion circuit 132 is also supplied to an on screen display control 127 of the MCC 104. The on screen display control 127 selectively generates on screen character and graphic displays in place of or overlaid on the video signal. The modulator 142 combines the video signal from the output of the on screen display control 127 and the audio signal from the output of the mute circuit 125 and converts the combined signal to the channel frequency selected by the microprocessor 128, such as channel 3/4 for NTSC. The combined and remodulated signal is supplied as an RF output to a television receiver in well known manner.

A control microprocessor 128 controls the overall operation of the subscriber terminal 40. The subscriber communicates to and controls the microprocessor 128 through an interactive user interface with an on screen display. The user interface includes a keyboard 122 on the front panel of the subscriber terminal 40 and the remote 126 which generate subscriber control signals for channel tuning, volume level control, feature selection, and the like. These subscriber control commands are decoded by an input scanner and control 148 of MCC 104. The remote IR receiver 124 of the user interface receives the commands from the infrared (IR) or other remote control 126, as

is well known in the art, and provides commands to the microprocessor 128. The user interface additionally includes a 4 digit, 7 segment LED display 120 which displays the tuned channel numbers and diagnostics.

When the keypad 122 or IR remote control 126 is utilized to select a command, the microprocessor 128 operates to execute the command. For example, this operation may be to instruct the tuner control 102 to appropriately control up/down converter 100 to tune a selected channel. The subscriber terminal interacts with the subscriber by providing numerous on screen displays which assist in the operation of the terminal. The on screen displays provide information and prompts to guide the subscriber through many of the complex features of the terminal.

The descrambler control 110 of the MCC 104 utilizes recovered descrambling data to generate appropriate control signals, for example, inversion control and equalizing, sync restoration or regeneration for descrambling, or otherwise restoring the input baseband television signal. A secure microprocessor 136 determines whether the descrambler control 110 of MCC 104 carries out descrambling on a particular channel or what form of descrambling is required at a particular time by interpreting the authorization and control data downloaded from the system manager 12 (by any of the three data transmission schemes discussed herein, out-of-band, in-band audio or in-band video) into the internal NVM memory of the device. The nonvolatile memory (NVM) in the secure microprocessor 136 stores secure data, for example, authorization data, scrambled channel data, scrambling mode data, some terminal configuration data and other required data.

The control microprocessor 128 operates by running a control program which preferably is partially stored in a read-only memory internal to the processor and partially stored in a non-volatile memory such as Flash EPROM memory 134. In addition, the control program of the control microprocessor 128 may also reside in the non-volatile memory of an expansion card 138. The microprocessor 128 communicates with the non-volatile memory 134 and 138 via a memory bus 141 which has data, address,

and control lines. In addition, the microprocessor 128 controls the data decoders 117, 129 and 146 and the tuner control 102, volume control 118, on screen display control 127, descrambler control 110 and input key scanner and control 148 via commands through MCC 104 and control microprocessor bus (CMB) 131. The microprocessor 128 also directly controls the mute switch 125 and the output frequency selection of the modulator 142. The microprocessor 128 includes additional capacity for other auxiliary device communications and control through a data port 140.

The memory control 112 permits data coming from the three data decoders 117, 129 and 146 to be placed in a volatile memory such as DRAM 137. There it can be accessed by the control microprocessor 128 via the CMB 131. The MCC 104 also distributes control instructions from the control microprocessor 128 to the other parts of the MCC 104 to provide operation of the rest of the subscriber terminal 40. The MCC 104 additionally connects to a secure microprocessor bus (SMB) 143 which permits communications between the secure microprocessor 136 and other portions of the subscriber terminal 40. The SMB 143 is further coupled to the expansion card 138 to provide renewable security.

The memory control 112 and microprocessor interfaces of the MCC 104 are the central communications facility for the control microprocessor 128 and the secure microprocessor 136. The memory control 112 receives requests to write to memory or read from memory from the microprocessors 128, 136 and the other controls and data decoders. It resolves contentions for memory transfers, giving priority to real time applications and the microprocessors, and schedules the data flow. The microprocessors 128 and 136 communicate through internal of the MCC 104 with the memory control 112 and other portions of the MCC.

The expansion card 138 is a printed circuit card which contains memory and/or secure microprocessor components, which can be plugged into a connector 200. The connector 200 electrically extends the control microprocessor memory bus 141

and the secure microprocessor bus 143 to the expansion card 138. Additional program or data memory, or renewed security can be provided by the expansion card 138.

The subscriber terminal may optionally include an impulse pay-per-view (IPPV) module of either the telephone type 152 or the RF-IPPV type 154. The IPPV module allows the subscribers to request authorization of their subscriber terminal 40 to receive pay-per-view events, store the data associated with the purchase of the event in the non-volatile memory of the secure microprocessor 136, and then transmit the data to the system manager 12 via the telephone return path or the RF return path via the signal distribution system 52.

The on screen display system will now be more fully described beginning with reference to Figs. 3-10. In Fig. 3, each on screen display can be generated as an array of pixels having up to 320 vertical columns and 200 horizontal rows. The 200 x 320 pixel size is chosen to generate adequate resolution for a standard NTSC receiver. Of course, other video formats, such as the several PAL formats, can be supported by adding additional pixels and lines. Additionally, different sized pixels forming other display areas can be provided for any television signal format. Each on-screen display is generated by the display controller 127 by producing analog pixels for the horizontal scan lines of the screen of the television receiver of the subscriber. The display controller 127, under the command of the control processor 128, controls the time of such display and which display to produce on the screen of a receiver.

The on screen display processor 127 operates on a video field by video field basis. A display screen is formed from display attributes and stored display data describing the screen or field in terms of pixels. This field can then be displayed in a noninterlaced form for nonvideo purposes or mixed in an interlaced form with active video. The field can be displayed many times to produce a static display, or the display parameters and display data can be changed to produce varying images. In either case, the on-screen display is activated by

a command from the control processor 128 and will continue to display a screen which is stored in the display memory until disabled by the control processor. This produces a particularly advantageous system when the control processor 128 and display processor 127 can operate in parallel without completely monopolizing control processor resources.

In this display environment, three types of display modes can be produced including a text or symbol screen mode, a graphics screen mode, and a combination mode where text and graphics screens can be displayed together. In addition, any of these modes can be used in combination with a border screen mode.

In the text or symbol screen mode, as seen in Fig. 3, the on-screen display is defined as a plurality of symbols, each symbol being of a variable pixel array of size m x n, where m = 6,7... 16; n = 6,7... 32 and m x n $\leq$ 512. By providing a variable size of symbol, many different types of symbol sets and sizes, such as different character fonts can be realized. Additionally, different foreign language character sets such as Japanese, Arabic, Chinese or others can be easily realized in this manner. A text screen can encompass the entire display array or be any size down to one symbol. Each text screen is defined by a vertical start and stopping point VSTART, VSTOP, and a horizontal starting and stopping point HSTART, HSTOP.

A preferred example for an English character set would be an 8x12 pixel array which would yield a maximum of 16 symbol lines on a text screen display with 40 characters per line. Another preferred example for a Chinese character set would be a 12x12 pixel array which would yield a maximum of 11 symbol lines on a text screen display with 26 characters per line. A plurality of these symbol arrays, each defining a particular character in a character set, are grouped in the display memory to form symbol set definitions, such as English, Chinese, font A, font B, etc. It is evident that the subscriber terminal 40 may store multiple symbol set definitions.

An example of a character from an English character set, a 8x12 pixel array, is illustrated in Fig. 9. The character has

a 1x8 pixel underline and a 1 pixel wide border around a 7x9 pixel character field. The character is defined by selecting pixels from the character field in a particular pattern. Each pixel of a symbol definition is stored as a 2 bit pixel attribute field which describes one of the four possibilities shown in the table of the figure. Each pixel can be either a foreground pixel, a background pixel, a black pixel or a white pixel.

To build a text screen display, a plurality of symbol pointers (each addressing a selected symbol in a symbol set definition) is stored in the sequence which the characters are to be displayed. For example, if the word LIST is to be displayed on the screen, then successively, the symbol pointers for the English character set elements L, I, S, T would be concatenated. The pointers may further contain symbol attributes for each character as in shown in the example for Fig. 8.

The illustration shows a symbol pointer as a 16 bit word which has a 7 bit symbol attribute field and a 9 bit symbol address. The 7 bit attribute field contains a 4 bit field defining the color of a character. These four bits may select one of sixteen colors of a color pallet register stored for that purpose. The other three symbol attribute bits include one bit to determine whether the character is to blink, another bit to determine whether the character should be underlined, and a foreground mode bit for special effects for the character.

In the graphics screen mode, the display system utilizes the entire 300x200 pixel display as a pixel mapped graphic as seen in Fig. 4. Each pixel can be displayed as one of the sixteen colors of the foreground or background color pallet memory. In the graphics mode, the color is then selected by 4-bits stored for each pixel.

For the combination mode as seen in Fig. 5, both the symbol screen mode and the graphics screen modes are used simultaneously. A graphics screen of less than the full screen is defined and displayed in the normal graphics mode. This display can then be overlapped with a text mode display which

does not display in the graphics window area. The reverse is also provided where a text screen can be overlayed on a graphics screen.

The display processor also includes a border screen feature where a border screen of a particular color may be placed around the graphics or symbol screens. The border feature is shown in exemplary form in Fig. 6 where the border pixels are active whenever the graphics screen and symbol screen are inactive and the border screen is enabled.

The color of the border screen is produced by loading a 12 bit color value in a border screen parameters register. The location of the border is set by loading the horizontal starting and ending locations, and the vertical starting and ending locations on the screen. The border screen may be disabled by storing a vertical start number which is larger than the maximum number of lines on a screen.

The display controller receives a number of display parameters which it loads into its control registers to regulate processing of the display function. The first set of display parameters is the screens heights and widths which can be at a maximum the full screen of a 320x200 pixel array and, if less than the full display area, the display screens locations. All those screens which will be active in the display area will have these parameters stored for them. The second set of parameters is a symbol set dimension nxm defining one of the symbol definition sets. As will be more fully discussed, multiple symbol definition sets can be stored and displayed in one screen.

The display system provides an extremely powerful and flexible tool for producing on screen displays for the subscriber terminal. The display system can be used in a text only or a full pixel mapped graphics mode only. The display can be a combination of text with a variably sized and variably positioned graphics window which itself is fully pixel mapped. The screens may be full sized or any smaller defined size for.

For a character or graphics display, thirty-two colors can be programmed for a character or pixels. The color palette

registers may be changed to display 16 choices for foreground and 16 choices for background from a 4096 choice color palette. On a per line basis a character set can be changed. On a per character basis selections for background and foreground color are available. Moreover, characters may take on border, underline, blink and highlight features on a selectable basis.

The display system provides a color palette of approximately 4096 colors which are defined as 12-bit digital words having a 4-bit luminance component, a 4-bit B-Y (blue-luminance) chrominance component, and a 4-bit R-Y (red-luminance) chrominance component. Combinations of these bits allow a user to select a wide variety of colors. Of course not all 4096 combinations of 12 bits will define useful colors, but there are a great number of useful hues and tints available.

The digital processor contains a plurality of palette registers as shown in Fig. 10 into which these colors can be stored. Any thirty-two of the colors can be stored at one time, as there are sixteen background color registers and sixteen foreground color registers. The system uses a 4-bit pointer to select one out of the sixteen colors for both foreground and background by pairing the registers. This feature is useful in providing a plurality of letters of one chosen color on a chosen background color, for example blue letters on a white background. This configuration can be programmed easily by the same color pointer for all letters indicating a palette register pair having a blue color loaded into the foreground register and a white color loaded into the background register.

A system block diagram of the on screen display controller 127 is more fully illustrated in Fig. 11. The on screen display controller 127 operates under commands from the control microprocessor 128 to provide on-screen displays for the subscriber terminal in the form of text screens, graphics screens, or combinations of text and graphics screens. The on screen display controller 127 comprises a two part display processor including an analog processor 300 and a digital processor 302.

The digital processor 302 receives commands and configuration data from the control microprocessor 128 over a bus 301 and video timing data 303 from the VBI decoder 129 indicating the start of each horizontal line and the start of each vertical field. The digital processor 302 uses the display parameters from the control microprocessor 128 to access display information in the DRAM 137 for the particular on screen display which is to be generated. The on screen display may be only text, and, in that instance, the symbol screen definition portion 305 and symbol set definitions 307 portion of the DRAM 137 are accessed. If the on screen display is only graphics, then the graphics screen definitions portion 309 of the DRAM 137 is accessed. If a combined screen of text and graphics is needed, then all three portions 305, 307, and 309 of the display memory are accessed.

The digital processor 302 accesses information in these portions of display memory on a nybble by nybble basis. It fetches data from the DRAM by its connections to the memory controller 112 through control lines, address lines and data lines 311. The digital processor 302 requests data from the DRAM 137 by providing a calculated starting address, number of memory locations accessed, and control commands to the memory control 112, and the data is returned over the data lines 311 and 313. The digital processor 302 processes this data to convert it into a series of digital words, each indicating the luminance and chrominance values of a pixel for the on screen display. These digital words which represent analog pixels, along with appropriate timing signals, are sent from the digital processor 302 to the analog processor 300 over timing and data lines 315.

As better illustrated in Fig. 12, the analog processor 300 includes a conversion means 314 to convert the digital pixel words to analog pixels. The analog processor 300 also receives the incoming video signal VIDEO IN, after its demodulation, and inputs the signal to one part of an analog multiplexer 316 which can select on a pixel by pixel basis, either analog pixels from the VIDEO IN signals or analog pixels from the digital to analog

pixel converter of the analog processor 300. The analog processor 300 selects which pixel to output based on a pixel select signal PIXSEL. The digital processor 302 generates the pixel select signal PIXSEL based upon whether the display processor is enabled and is outputting a valid color definition.

The digital processor 302 causes the pixel select signal PIXSEL to choose the VIDEO IN signal if both of these conditions are not met. The multiplexed output is then output to the modulator 142 as the VIDEO OUT signal. The analog processor 300 further generates the pixel clock signal PIXCLX from a oscillator clock CLK. This is the basic training signal of the display processor and divides a horizontal line with 455 pixels of a duration of approximately 139 nanoseconds each. If the pixel clock is needed for display during a time when no VIDEO IN signal is tuned by the subscriber terminal, then it is generated directly from the oscillator clock signal CLK. This is a so called internal video mode. If the pixel clock is used for a display where the video signal is present, then it is generated by phase synchronization with the horizontal sync of the VIDEO IN signal by a sync slicer 291 and a phase locked loop 293.

The digital processor 302 is controlled by the control processor 128 by reading and writing the registers R1-R12 shown in Fig. 14. The display attributes for the on-screen display can be controlled by loading and reading particular registers in the digital processor 302.

The type of screens which can be displayed and their location on the display area of the television receiver are provided by a border screen parameters register R2, a symbol screen parameters register R4, and a graphics screen parameters register R5. All of the screen registers have information concerning the horizontal starting point (SH) and stopping point (EH) and the vertical starting point (SV) and stopping point (EV) of each of the respective screens.

A symbols screen or graphics screen can also have associated with it the starting memory locations of where the display information is stored in DRAM 137. This information is

loaded into the symbols screen base address register R8 for the symbol screen, and the graphics screen base address register R9 for the graphics screen. Because the border screen is generated internally and not stored in the DRAM 137, register R2 also contains a 12 bit digital word describing the color of the border screen. All pixels of the border screen are generated from this color.

To activate the symbol screen, the graphic screen or the border screen, the starting address of the screen must be within the display area limits. Conversely, to deactivate any of the screens, the vertical starting address of a respective screen is set to a line number outside the display area. A control bit CONTR is used in register R2 to enable and disable the function of the screen border.

The colors for a selected pixel of a screen can be chosen by one of the color registers R6, R7 and R10. There are sixteen foreground palette registers and sixteen background palette registers R10, a black color register R6, and a white color register R7. Each of these registers is capable of storing a 12 bit color as described for the palette section, 4 bits of luminance and 4 bits each of the two phases of chrominance.

There are two sets of registers R11 and R12 which provide control of the symbol line attributes. Each symbol line in a symbol screen display can be of a different font or style which is defined as a symbol set definition in the display system. There are up to sixteen symbol lines, and each of these can have a number of line attributes which are stored in sixteen symbol line attribute registers R11. The first field of a symbol line attribute register is the address of one out of four symbol set definition registers R12. The second field is a one bit line attribute, which selects either the foreground or background color for the underline color. The particular color palette register chosen is then described in a 4-bit field, palette register. Additionally, a special effects bit ULI for inverting the luminance for the underline is provided where, if the bit is cleared, the luminance of the underline is provided normally,

and if the bit is set, the intensity of the luminance of the underline is inverted.

The two bit symbol line definition in the line attribute register R11 selects one out of four symbol set definition registers R12. Each symbol set definition register R12 stores the size of a particular symbol set, m x n, the number of nybbles in a symbol, and the symbol definition base address. Registers R12, along with the symbol line attribute registers R11, allow up to four different types of symbol set definitions to be used simultaneously in the display system.

The last two registers that are provided are for control and selection of different functions of the display processor. The first is a video parameters register R1 and the other is a control parameters register R3. The video parameters register R1 defines the control timing of the particular video signal that is to be generated by the display processor. The horizontal sync start time SYNC S and end time SYNC E are stored along with the vertical synchronization start time VSYNC S and end time VSYNC E. Also defined are the color burst start time CB S and end time CB E. To time the vertical blanking interval, the equalizing pulse start time EP S and end time EP E are also stored in the video parameters register R1.

The control parameters register R3 is a two byte register which stores a number of control bits choosing the modes and features for the display processor. The blink rate BR for symbols and underlines is stored in increments of .25 seconds from 0-4 seconds. The blink duty cycle BD can be set with two bits indicating duty cycles of 25%, 50% or 75% on and conversely 75%, 50% or 25% off. The blank screen bit BK can be used to blank a screen, if set to 1, or to display the screen normally, if set to 0. Further, an internal/external selection bit INT is used to determine whether the video signal is to be internally generated, if set to 1, or synchronized to the external video signal, if set to 0.

If the signal is being internally generated and is not being synchronized to an interlaced video signal, then an interlace control bit ILC can be set for non-interlaced fields

or cleared for interlaced fields. Two further fields, PALFOR and PAL/NTSC, are used to select either the NTSC or PAL format and, if PAL format, the type of PAL format which is to be selected. The bit GSEL is used to select whether the color palette for graphics is the foreground palette or the background palette. The control bit EN is used to enable the on screen display controller or disable the on screen display controller. The underline blinking bit UNB indicates whether the underline of a symbol will blink or not blink. Four bits for an upper address field UA are used to allow the digital processor 300 to extend the size of DRAM 137 which it can normally address. The control bit PR is used to indicate whether a symbol screen has priority over a graphic screen, or if the graphic screen has priority over the symbol screen.

To display a screen, a screen display routine from the executable code is called for execution by the control processor 128. The screen display routine will move the particular screen information which it is programmed to display from the nonvolatile memory (ROM or flash EPROM) to the display memory area of DRAM 137. The screen display program can then disable the digital processor 300 by clearing the enable bit EN to load the processor registers R1-R12 with the desired display attributes. Normally, the screen display routine will only disable the display of the digital processor 1302 by setting the blank bit BK if it needs to only reload the palette registers or line attribute registers.

The control processor 128 need not load all the processor registers because it can read them to determine if any changes are actually needed. For example, once the video parameters register R1 and most of the control registers R3 have been programmed once, they will not often need to be changed. Likewise, the color registers R6, R7 and R10, after they have been set up with the desired palette of colors, will remain relatively unchanged for many display scenarios. Moreover, because four different symbol set definitions or fonts can be used simultaneously, the line attribute and symbol set

definition registers R11 need not be changed for every scene change.

The most likely registers to be changed are the registers R8 and R9 to indicate to the digital processor 300 where the screens are to found in the DRAM 137. The next most likely registers to be changed are the screen parameter registers R2, R4 and R5 which position the different screens on the display area.

After the control processor 128 has set the display attributes in the registers R1-R12 to the desired display configuration, it will re-enable the digital processor 300 by setting the enable bit EN or clearing the blank bit BL to display the stored screens until the device is thereafter again disabled, or the display information or the configuration information is changed.

A more detailed block diagram of the digital processor 302 is shown in Fig. 13. The digital processor 302, under the command of the control processor 128, generates the digital pixels for an on screen display from information stored in the DRAM 137. The on screen display can be programmed with a number of attributes which will change its appearance by programming the digital processor 302 with the commands from the control processor 128. In general, the digital processor includes a synchronizing circuit 304, a control interface circuit 306, a memory interface and timing circuit 308, an address generation circuit 310, and a pixel generation circuit 312.

The synchronizing circuit 304 has two modes of operation, internal and external. When in external mode, the circuit 304 receives a timing signal Hs from the VBI decoder 129 and uses it to synchronize the operation of the display processor to the VIDEO IN signal. The Hs signal is also passed to the pixel generation circuit 312 and other circuits to provide basic timing information. The Hs signal is synthesized by the VBI decoder circuit 129 from the incoming video signal to provide a one clock pulse wide (24 Mhz) signal at the initiation of every horizontal line, and a clock pulse of two clock pulse widths at the beginning of field one, at line one, of a

television signal. From the Hs signal, the pixel clock signal PIXCLK, and data from the control interface circuit 306, the synchronizing circuit 304 provides the pixel number of a particular horizontal line and the horizontal line number of the present video field.

These timing signals are provided to the other circuits of the display controller to produce pixel time base. The timing signal Hs resets the pixel line number, and the extended timing signal Hs resets the horizontal line number to a predetermined starting line. When operating in internal mode, the synchronizing circuit 304 generates the timing signals from the pixel clock signal, PIXCLK without synchronization to an external video signal. In addition, whatever the mode, timing pulses are generated indicating the positions of the horizontal sync time, sync tip time, the color burst time and equalizing pulse time to permit the pixel generation circuit 312 to insert the appropriate signals in the video output.

The control interface circuit 306 provides a means for the control processor 128 to access the configuration registers R1-R12 of the digital processor 302. The circuit 306 decodes the operational commands, OpCode and addresses ADD of the control microprocessor 128 to determine which configuration register is to be read or written, and with what data. To provide the configuration data and to read the status of the digital processor 302, the control interface circuit 306 has an 8 bit data bus DataIN coupled to all of the configuration registers for the write operation, and an 8 bit data bus DataOut coupled to the output of all of the configuration registers R1-R12 for the read operation. The outputs of the configuration registers R1-R12 are then used to provide control signals and configuration data to the other circuits.

The address generation circuit 310 and the memory interface and timing circuit 308 operate cooperatively to fetch display data from the DRAM 137 and supply it to the pixel generation circuit 312. In this regard, the address generation circuit 310 will calculate the beginning address of a block of data OsdADD. The memory interface circuit 308 registers the memory transfer

with the osd REQ signal and will assert the signal osd A during active video times. The memory interface circuit 308 will also generate the number of bytes OsdN to be fetched from the DRAM 137. Each byte will be acknowledged when sent with an signal ACK from the memory controller 112 and the data delivered over a 4 bit bus osdDATAOUT directly to the pixel generation circuit 312.

When the memory controller 112 has finished its transfer, it will alert the memory interface 308 with a signal osdD. If the pixel generation circuit 312 is receiving more data than it can display, then it will request a suspension in the memory transfer cycle from the memory controller 112 by asserting the pause signal osdHOLD. The memory controller 112 will pause in response to the signal and not resume the transfer until the signal is osdHOLD disabled.

The pixel generation circuit 312 receives the timing data from the synchronizing circuit 304 and the display data from the DRAM 137 via the memory controller 112 and converts the data into digital pixels for the analog processor 300. The display data is properly displayed by modifying it by the various configuration data which has been stored from the control processor 128 in the plurality of configuration and control registers R1-R12.

The detailed schematic diagrams for the digital processor 302 are illustrated in Figs. 15-20 and will now be more fully explained by reference thereto.

Figs. 15 and 16 illustrate a detailed schematic circuit diagram of the synchronizing circuit 304. With respect to Fig. 16, in response to the pixel clock signal PIXCLK and the horizontal synchronizing signal Hs from the VBI data decoder circuit 129, the synchronizing circuit 304 generates the basic horizontal and vertical timing signals for the display system to the other processor circuits. The timing signals can be internal which are synchronized to a derived time base or external which are synchronized to the VIDEO IN signal.

The synchronizing circuit 304 comprises a pixel counter 205 and a horizontal line counter 213. The pixel counter 205 is

incremented on the time base of the signal PIXCLK to count to 455, which is the number of pixels in each horizontal line. The comparator 207 senses the output of the counter 205 and compares it to 455. A reset signal RES is output from the comparator 207 when the pixel counter 205 reaches that number of pixels. This reset signal is used as one input to a multiplexer 203 to indicate the internal horizontal line duration.

The multiplexer 203 also receives another input from the horizontal synchronizing signal Hs to provide an indication of when the counter 205 should be reset at the beginning of an external horizontal line. Alternatively, if the time base of the circuit is to be generated internally the internal bit signal INT/EXT from the control register selects the output of the comparator 207 to reset the pixel counter 205. The output of the multiplexer 203 is further used to generate the horizontal sync signal HSYNC signal to the other circuits which, depending upon the internal bit signal, can either be the signal Hs or the output of the comparator 207. The internal signal INT/EXT is generated by the setting or cleaning of the bit in the control register. In general, the external synchronization of a video signal is used but, when no video signal is present, the internal bit is set by the control processor 128. The situations where no video signal will be present are on power up, menu display, some pay per view functions, changing channels, etc. The control processor will sense this status and set the internal bit to provide a time base for the display despite the lack of a video signal.

The vertical synchronizing signals are generated similarly. The horizontal line counter 213 basically counts the number of horizontal lines in a field and then is reset at the beginning of the next field. The multiplexer 209 outputs a signal which increments the counter 213 for each horizontal line. One of the inputs to the multiplexer is the external horizontal synchronizing signal Hs and the other input is the output of the comparator 207 from the internally generated horizontal line count. The time base selection signal INT/EXT then selects

between these two inputs to increment the counter 213 for each horizontal line.

The reset signal for the counter 213 at the beginning of each field is provided by the output of a multiplexer 211. For an external reset of the counter 213, a pulse width detector 201 detects the two clocks wide pulse of the VBI data decoder circuit 129 which indicates that the timing of the external video signal is beginning field one, line one. The other input to the multiplexer 211 is an internally generated field number which is the output of multiplexer 219. The time base selection bit INT/EXT is used to select between these two reset signals.

The internally generated field numbers are provided by the outputs of the comparators 215 and 217 which have one input connected to the output of the counter 213, and their other inputs connected to a predetermined number of horizontal lines 263 and 262, respectively, for an NTSC signal. The output of the multiplexer 219 generates its own select signal via the output of a D bistable 221. The output clocks the bistable 221, which has its *Q output coupled back to the D input of the device. The selection signal alternates between the inputs of the multiplexer 219 to select between the alternate fields of an internally generated video signal having fields of 263 lines, as detected by comparator 215, and 262 lines, as detected by the comparator 217. The D-bistable 221 is disabled from the alternate selection of the two fields by the NAND gate 220 which stops the feedback. In this mode only one field, field 1, is generated by the synchronizing circuit 304. The gate 220 is disabled and enabled by the control bit ILC which produces an interlaced (2 fields) display if in one state and a non-interlaced (1 field) display if in the other state.

The horizontal line number then is output from the counter 213 to the other circuits along with the vertical synchronizing signal VSYNC from the output of the multiplexer to 211.

Fig. 15 shows a detailed schematic of the portion of the synchronizing circuit 304 which generates the video mode signals to the pixel generation circuit 312. The video mode signals are to partition the video signal into three portions and to time

the actual generation of pixels for the on screen display. The first portion is an active video portion which corresponds to a normal active video section of a horizontal line extending from the back porch of the horizontal blanking pulse to the front porch of the next horizontal blanking pulse. In the present embodiment, this active video is a predetermined number of pixels in length where each pixel is 139 nanoseconds. The video mode signals further provide a group of signals which define the horizontal and vertical blanking signals, the active video portions, and the retrace intervals. The decoding logic 399 generates the video mode signals to the pixel generation circuit 312 by decoding four video active signals from bistables 392, 394, 396 and 398.

The sync tip active signal is the output of the bistable 392, which is set by a comparison between data indicating the start of a sync tip from register 360, and the pixel number from the sync circuit 304. The sync tip active bistable 392 is reset by a comparison between the pixel number and the sync tip end register 362. The color burst active signal is generated as the output of a bistable 394. The color burst active bistable 394 is set by comparator 380 which compares the value of the color burst start four register 364 with the pixel number. The bistable 394 is reset by a comparison between the pixel number and the contents of the color burst end register 366.

The video line active signal is produced as the output of a bistable 396. The video line active bistable 396 is set by comparator 384 from a comparison between the contents of H video start register 368 and the pixel number. The bistable 396 is reset from the output of a comparator 386 which determines when the contents of the H video end register 370 matches the pixel number. The fourth active signal is the active field signal from the output of a bistable 398. The bistable 398 is set by comparison between the contents of the V video start register 372 and the horizontal line number from the sync circuit 304. The bistable 398 is reset from the output of comparator 390 which compares the horizontal line number with the contents of the V video end register 374. The active video signals define

the timing of a field of an NTSC signal, or other video formats, into pixels and horizontal line numbers. By preloading the registers with suitable parameters, most timing formats and protocols for a video signal can be programmed into the display controller.

Fig. 17 illustrates a detailed schematic of the control interface circuit 306. The control interface circuit 306 provides the electrical and logical data path connections between the digital processor 300 and the control processor 128 so that the latter can control and configure the former. The control interface circuit 306 provides the control signals and data from the control registers R1-R12 to the other circuits of the digital processor. Input of the control and configuration data to be stored in the registers R1-R13 is via an 8-bit data bus, DataIn which is connected to the data inputs D of all the registers R1-R12.

The command signal, Opcode, and the address signal, ADD, from the control processor 128 indicate which byte of which of the registers R1-R12 is to be read or written. The write operations for the registers are decoded by a decoder 231 which selects the correct registers and byte with a plurality of output control lines. Each of the output control lines are connected to the write inputs W of the registers R1-R12 through a plurality of AND gates 233. The other input to the AND gates 233 is the control processor write signal Pwrite.

The control processor 128 can write any of the positions in the registers R1-R12 by selecting the memory location where the data is stored, providing the data on the input bus, and then causing the write operation to occur by generating the signal Pwrite. In this manner, the control processor 128 can configure or change the registers in the digital processor 302 at any time. Once the digital processor 302 is configured, the control processor 128 can enable the device to generate the display and return to other control processing. This permits an extremely fast control of the digital processor 302 without requiring the control processor 128 to dedicate all of its resources to display processing.

The control processor 128, when it is desired to configure the digital processor 302, is not required to use the write process because the control processor can also read any of the outputs of the registers R1-R12. With a memory read operation, the control processor 128 can test to determine if the configuration is already that which is desired. The read process is produced by coupling all of the outputs of the registers R1-R12 to the inputs of a multiplexer 239. Any particular byte of a register which is to be read can be provided by decoding the command signal Opcode and address signal ADD at the selection inputs of the multiplexer 239. This will select one of the bytes of the registers R1-R12 for output on an output data bus, DataOut, through a group of a tri-state buffers 241. The tri-state buffers 241 are enabled by the control processor read signal Pread. The control processor 128 can read any output from the registers R1-R12 by selecting the byte and, when it is ready to read the data on the bus DataOut, by enabling the tri-state buffers 241 with the signal Pread.

The palette registers R10 and the line attribute registers R11, in addition to having data input lines and write enable lines, also include address lines A because they are groups of registers implemented in random access memory. The address of a particular register of the group is selected from the output of the multiplexer 245 for the palette registers R10. Normally, the address is selected by the color selection bits of a symbol pointer. However, if the control processor 128 wants to write a register of the palette registers R10, it must load the address of that register in an index register 235 which is the alternative input of the multiplexer 245. The Pwrite signal then will cause the multiplexer 245 to select the contents of the index register 235 as the address when writing information into the palette register R10 from the bus DataIn.

A similar method is used to write the line attribute registers R11 with the output of a multiplexer 247 connected to the address selection lines A of this memory. Normally, the symbol line number from the symbol line counter will be used to address the registers R11. However, if the registers R11 are

to be written by the control processor 128, the address is selected by an index register 237 which can be loaded through the bus DataIn. One output of the line attribute registers R11 is the selection of the symbol definition from the symbol set definition registers R12. The definition of the symbol set is used for the selection inputs of a multiplexer 243 which chooses one out of the four symbol set definition registers R12.

The outputs of the registers R1-R12 are used by the other circuits to provide the parameters needed for the control of the display and the control signals needed to select different modes for the, display processor. The total information concerning the display is stored in the registers R1-R12 and form a display configuration which is variable depending upon the display attributes stored in the particular registers.

With regard to generating timing signals for determining when each type of screen is active, reference is given to Fig. 18. In the control interface circuit 306 there are 12 registers 320-331 which indicate the boundaries and locations for each of the three types of screens. Registers 320-323 store information concerning the vertical start and end, and the horizontal start and end, respectively for border screens. Registers 324-327 store information concerning the vertical start and vertical end, and horizontal start and end information for symbol screens. Registers 328-331 store information concerning the vertical start and end, and horizontal start and end information respectively for the graphic screens.

Logic including comparators 332, 333 and a bistable 344 determine from this information and the horizontal line number whether the border screen has stopped and started vertically. Bistable 344 outputs a high logic level from the beginning line number of a border screen to the end line number of a border screen. Likewise, bistable 345 decodes whether a border screen is active horizontally. The comparators 334 and 335 compare the contents of the registers 322 and 323 to the pixel number and output a high logic level from the bistable 345 if the pixel number is between the horizontal start and end of the border screen. A combination of the high levels from bistables 344 and

produce a border screen active signal from the output of an AND gate 349. In a similar manner, AND gate 350 develops a symbol screen active signal from the outputs of bistables 346 and 347. The bistable 346 is set to a high logic level between the vertical start and end of a symbol screen. The comparators 336 and 337 compare the contents of registers 324 and 325 to the horizontal line number to set and reset the bistable 346. The horizontal extent of the symbol screen, which is stored in registers 326 and 327, is with the assistance of comparators 338 and 339 used to set and reset the bistable 347. A high level output from the bistable 347 indicates that the pixel number is between the horizontal starting position and the ending position of the symbol screen.

In an identical manner, the AND gate 351 develops a graphic screen active signal from the outputs of bistables 348 and 348a. The bistable 348 is set at the vertical start of the graphic screen and is reset at the end of the graphic screen. The bistable 348a is set at the beginning of the horizontal start of the graphic screen and is reset at the horizontal end of the graphic screen. Comparators 340 and 341 set and reset the bistable 348 by a comparison between the horizontal line number and the contents of registers 328 and 329, respectively. The bistable 348a is set and reset by comparators 342 and 343 comparing the pixel number to the horizontal start and end contents of register 330 and 331, respectively.

These signals are combined in logic 352 with a priority signal from a priority control circuit 352a to indicate to the address generation circuit 310 from which portion of memory pixel data should be selected. The general rule is the symbol screen and the graphic screen both have priority over the border screen. Thereafter, the graphics screen or symbol screen will have priority depending on the configuration data stored in register R3 for the priority bit PR. This permits a symbol screen to be overlayed on a graphics screen or vice-versa.

Fig. 7 illustrates symbol screen which has priority. When pixels in the symbol screen are active, display data is fetched for it rather than the graphics screen. Another priority

determination is made to check if the blanking bit BK is set in the control register. The blanking bit will take priority from both other screens and essentially blank the screen by displaying the border screen. This will allow a smooth transition between channels and other states where a symbol screen, a graphics screen, or active video is inappropriate. In addition to this priority determination, if the symbol and early signal is generated to logic 352, the display processor will fill in end spaces with the border pixels of the color selected. This also occurs for the border screen pixels, if there is a gap between a symbol screen and a graphics screen.

The symbol end early signal is generated from an OR gate 357 which has inputs from comparators 354 and 356. Adders 353 and 355 provide one input for the comparators 354 and 356 and the other is the line number and the symbol size. The other input into the comparators is the horizontal end signal for the symbol.

The timing circuit 308 further produces a next line signal to the pixel generation circuit 312 as the output of a comparator 359. The comparator 359 compares the contents of a symbol line counter 358 with the cube height (n). The symbol line counter 358 counts the lines of a symbol by its incrementation from the horizontal sync signal HSYNC from the syncronization circuit 304. When the symbol line counter is equivalent to the cube height in horizontal lines, it is reset to zero for the next symbol.

The timing circuit 308 generates a data path select signal to the pixel generation circuit 312 as the output of a symbol pixel counter 318. The symbol pixel counter is compared with the cube width (m) in a comparator 319 and, when the counter reaches the extent of the symbol width, the counter 318 is reset. The counter 318 is clocked by the pixel clock signal PIXCLK.

The last signal that is generated by the timing circuit 308 is the next graphics pixel signal which is directed to the address generator circuit 310. The next graphics pixel signal is the output of an AND gate 315. The inputs to the AND gate

315 are the coincident combination of the graphics active screen signal (from AND gate 351) and the pixel clock signal, PIXCLK.

Fig. 19 is a detailed electrical schematic of the address generation circuit 310. The address generation circuit 310 generates DRAM addresses for three different types of data. The data, as has been explained previously, consists of graphics data, symbol data, and pointer data from the three areas of display memory. A multiplexer 423 selects between one of these address generators to generate the addresses of the particular data which is to be output to the DRAM 137. The address selection signals from the timing circuit 308 cause a pointer to be addressed, and then cause the symbol pointed to be addressed during a symbol screen display. Alternatively, a graphics address generator is used to address bytes from the DRAM 137 for a graphics screen display.

A pointer is addressed by the output of a pointer register 431. The pointer register 431 is initially loaded on the start of a video field (VSYNC) with a symbol base address. The symbol base address is the address of the first pointer for a symbol screen definition. This is done through one path of a three input multiplexer 429 upon the occurrence of the VSYNC signal. Pointers are addressed in this stored sequence by adding 4 nybbles for every cycle with an adder 425 which is another input to the multiplexer 429.

After a pointer address is calculated, the symbol which it points to is addressed. The data in a pointer enters from the osdDataOut path into a symbol number register 403 where it is multiplied by the symbol size in a multiplier 417. The symbol number times the symbol size when added to the symbol base address in an adder 419 yields the address of the first nybble of the symbol. This symbol data is then input symbol line by symbol line by the multiplexer 423 by adding a symbol line offset from line offset to adder 421 register 415. The line offset 415 is loaded from the next line timing signal which is the addition of the previous line and the symbol line width from an adder 413.

The graphics addressing is accomplished by a graphics pointer register 409 which is loaded through multiplexer 407 from the graphics base address register will then VSYNC signal. The graphics pointer register will then contain the address of the first byte of the graphics screen area. The multiplexer 407 is then switched to the output of an adder 405 which adds one byte to the graphics pointer register 409 for every pixel clock to sequence through the graphics addresses of the DRAM 137. The graphics pointer register 409 is incremented by the next graphics pixel signal from the timing circuit 308.

Fig. 20 illustrates a detailed schematic of the pixel generation circuit 312. The pixel generation circuit 312 is basically a circuit which generates a 12-bit digital word representative of the analog value of a pixel at a particular point in the video field. It comprises two multiplexers 381 and 383 which produce 12-bit digital words which are then output to the analog processor 300. The multiplexer 383, in response to the video mode signals from the sync circuit 304, selects either from a group of fixed values which are stored in locations 361-367 of a memory (preferably ROM) or the output of multiplexer 381. The values stored in memory locations 361-367 are digital representations for the analog blanking level 361, the internal color burst level 363, the external color burst level 365 and the sync tip level 367. During horizontal and vertical blanking intervals, these values are used to produce the analog levels necessary to output a video signal to the television receiver.

During the active video portions of horizontal lines, the multiplexer 381 is used to select between six 12-bit registers which contain the colors of a particular pixel. The multiplexer 381 can select between a color (white) from register 369; or a color (black) from register 371; the foreground palette 373 (consisting of 16 registers) or the background palette 375 (consisting of 16 registers). Otherwise, a pixel color can be provided from a border color register 377 which stores a chosen color for the border screen. Alternatively, a color from the underline palette register 379, can be selected.

The selection of one of these colors is made by the multiplexer 381 from the multiple states of a selection signal from combinational logic 397. The combinational logic 397 decodes the two bit pixel attribute data in each of the pixels of the symbols to pick one out of the four choices for registers 369, 371, 373 or 375. The border register color is chosen when the border screen active signal is set. The underline palette color in register 379 is selected when the underline bit for a particular symbol is set during the last line of a symbol.

Data is input from the DRAM 137 through a register 403 which receives 4 nybbles and combines them into a 16-bit digital word. Thirteen bits of the 16-bit words are written into a FIFO buffer 405 which is thirteen bits wide and 8 words deep. The combinational logic 397 reads nine of the thirteen bits of the digital words to provide its selection logic. The other four bits of each word are directed to the palette registers to select one out of the sixteen foreground and background palette registers 373 and 375.

The output of the pixel generation circuit 312, whether it is an active video line, a sync time, or a retrace time period is a 12-bit digital word describing a color (4-bits Y, 4-bits R-Y, and 4-bits B-Y). The 12-bit digital words are multiplexed into a series of 8-bit digital word pairs by a multiplexer 385. The 8-bit digital words are stored as four bits of Y and four bits of either R-Y or B-Y. This is because the chrominance is at half the frequency of the luminance and this allows the output of the luminance value twice for every chrominance value.

Multiplexer 385 is selected with a clock signal from the output of a bistable 395 which is clocked from the pixel clock signal, PIXCLK. The output of the bistable 395 is inverted via inverter 393 and input to the D input of the device. This provides a clock signal at one-half of the pixel clock rate which alternately loads either the 4-bit values of R-Y or B-Y into the input of a FIFO buffer 387. The select signal from bistable 391 is input to the FIFO buffer 387 to identify which value is being transmitted.

The first 8-bits of output of the FIFO buffer 387 is to a multiplexer 389 which produces a 4-bit output from the 8 bit digital words coming from the buffer 387. The words for one-pixel are the luminance value in one four bit word and one of the chrominance value. The next pixel is the luminance value and the other chrominance value. These are sent to the analog processor 300 as PIXD at the pixel rate by the clock provided by bistable 391.

Bits 9 and 10 output from the FIFO buffer 388 are the pixel select signal PIXSEL which determines whether the analog processor 300 outputs a display processor pixel or one from the VIDEO IN signal. PIXSEL is multiplexed with each 4-bit output word and with the luminance indicates whether the pixel is a display pixel or an active video pixel and with a chrominance value indicates whether the value is B-Y (1) or R-Y (0).

For the pixel choice situation of PIXSEL, an AND gate 437 detects the coincidence of two conditions. The first is the presence of the enable bit EN set in the control register R3 indicating the display processor should be active. The second condition is the detection of a valid color by a transparent color detection circuit 439. In the present implementation, all colors are valid except those colors which are designated as transparent. A transparent color is defined as one, as detected by comparators 431, OR gate 433, and NAND gate 435, where the luminance value Y is zero, and either of the chrominance values B-Y or R-Y are nonzero. Therefore, the pixel select signal PIXSEL is a zero state when the display processor is disabled, such that the zero state selects the VIDEO IN signal pixel. When the display processor is enabled and a valid pixel color is detected, the state will change to one to choose the output pixel of the display processor. When the display processor detects a transparent color, even when enabled, the state of PIXSEL will be zero to produce a selection of the VIDEO IN signal pixel and an active video background pixel for a display.

The digital to analog pixel converter 314 and multiplexer 316 of the analog processor 300 is shown in a detailed schematic in Fig. 21. A balanced VIDEO IN signal for common mode

in Fig. 21. A balanced VIDEO IN signal for common mode rejection is input to one port of the analog multiplexer 414. The other port of the analog multiplexer 414 is a balanced analog signal from the pixel conversion circuit 314. The pixel conversion circuit 314 receives the 12-bit digital pixel words from the digital processor 302 and converts them into analog pixels which can be selectively substituted for the analog pixels of the VIDEO IN signal. The selection is controlled by the pixel select signal PIXSEL, which connects one of the input ports of the multiplexer 414 to the output port for one state and connects the other input port of the multiplexer 414 to the output port for the other state. The balanced output of the multiplexer 414 is linearly amplified in an amplifier 416 before being transmitted to the modulator 142 as the VIDEO OUT signal.

The pixel conversion circuit 314 performs a digital to analog conversion process where a digital pixel representing the luminance and chrominance of a pixel is converted into the analog equivalent of that pixel. The conversion circuit 314 includes a luminance digital to analog converter (LDAC) 410 and a chrominance digital to analog converter (CDAC) 400. The LDAC 410 converts the 4-bit luminance digital word Y into a DC voltage pedestal which is output in a balanced configuration to one input of an analog summation circuit 412. The CDAC 400 converts the 4-bit chroma word R-Y and 4-bit chroma word B-Y into a sinusoidal signal having a frequency of 3.58 Mhz and having a representative color phase with respect to the burst of the incoming VIDEO IN signal depending on its value.

This is the conventional chroma modulation which, when summed with the luminance pedestal in the summation circuit 42, will provide an analog pixel which can be substituted for an analog pixel of the VIDEO IN signal. The CDAC 400 generates the sinusoidal signal by converting the digital value of the R-Y and B-Y signals into a phase representation which varies with the phase of an incoming digital clock PH1-PH4, which is referenced to the color burst of the incoming VIDEO IN signal but is 4 times its frequency. The digital representation of the sinusoid at the correct phase is output from the CDAC 400 to a level

adjuster and amplifier 404 which references the digital signal to video ground. The balanced output of the level adjuster 404 is buffered by a linear buffer amplifier 406 before being input to a shaping filter 408. The shaping filter 408 comprises a network of frequency responsive elements such as capacitors and inductors. The shaping filter 408 acts to convert the digital representation of the sinusoid to an analog sine wave without varying its phase. The shaping filter 408 is essentially a low pass filter with steep roll off which removes the high frequency edges of the digital signal above 3.58 Mhz burst frequency.

A comparator 402 provides a level adjustment signal for the output voltage range of the outputs from the CDAC 400. This level compensation equalizes the level input to one port of the comparator 402 from the VIDEO IN signal with the level input to the other port of the comparator 402 from the output of the conversion circuit 314. The level compensation signal is used to adjust the maximum and minimum levels for the range of analog voltages generated by the CDAC 400.

The data flow for the display of symbols can be more fully understood with respect to Fig. 22. At the beginning of the display of a screen, the horizontal and vertical starting points and the horizontal and vertical ending points of the screen have been loaded into the appropriate registers. Further, the symbol screen base address register has been loaded with the address of the first symbol pointer in the symbol screen definition. The symbol screen definition consists of a plurality of these pointers which are stored in the DRAM 137.

The digital processor 302 when commanded by the control processor 128 to display the symbol screen fetches the first pointer 500 from the DRAM 137. The pointer 500 contains the symbol number 508 of a symbol definition set which is sent to the pixel address calculation process of the address generator 310. The pointer also contains the choice 510 of the palette register which is transferred to the pixel generation circuit to select the one of sixteen palette register 512 combination choices available. The bits F (foreground mode), U (underline), and B (blink) are sent to the pixel generation circuit 312 for

the different selections of these features. Additionally, the digital processor 302 determines from the symbol line counter the screen line number 514 which indicates which of the line attributes registers 516 should be chosen. The line attributes registers 516 have been previously programmed to select between up to four different types of symbol definition sets 518, and the color of the underline 520, if any, for the symbol. These particular line attributes are fetched and the color of the underline 520 sent to the pixel generation circuit 312 to select one of the sixteen colors of either the foreground or background palette registers 512.

The symbol set definition choice 518 is sent to the symbol set definition registers 522 and the symbol definition choice read out. The symbol set definition registers 522 contain the size of the symbol m x n 524 and the number of nybbles 526 it takes to store each symbol. The symbol definition register 522 also contains the base address of the symbol set definition 528 which, when added to the symbol number 502, will give the starting address of the particular symbol chosen for the display. The pixel address calculation process 530 causes the symbol 532 to be transferred from the DRAM 137 to the pixel generation circuit 312 where it can be applied to a multiplexer 534 having a number of inputs from the color registers 512, 536, 538, 540, and 542.

As the pixel attribute data for each pixel are read from the symbol 532, the two bits are decoded to select either the 12 bits of the foreground color, the 12 bits of a background color, the 12 bits of the black color, or the 12 bits of the white color. This normal selection process is modified by the F, U, and B bits which cause modifications of the normally selected colors.

The foreground mode (F) bit, if set, inverts the luminance (first 4 bits) of a chosen foreground color. The blink bit (B), if set, inverts the choice of the foreground color and background color during a configurable portion of the blink cycle. The underline bit, (U), if set, causes the last line of pixels in the symbol 532 to be output as the underline color

542. The pixels for each symbol 532 are read in sequence and the selection process continues until all the pixels of a particular symbol have been displayed. The digital processor 302 then returns to fetch another symbol pointer 501 from the symbol screen definitions 503. The fetching of the pointers and the display of the symbols continues in sequence until all of the symbols for the symbol screen definition 503 have been displayed.

The data flow for the display of a graphics screen will now be more fully explained with reference to Fig. 23. At the beginning of the display of a screen, the horizontal and vertical starting points and the horizontal and vertical ending points of the screen have been loaded into the appropriate registers. Further, the graphics screen base address register 550 has been loaded with the address of the first nybble 552 of the symbol screen definition. The graphics screen definition 554 consists of a plurality of nybbles that are stored in DRAM 137, each corresponding to one of the pixels of the graphics display. The digital processor 302 when commanded by the control processor 128 to display a graphics screen fetches the first nybble 552 from DRAM 137 and transfers it to the pixel generation circuit 312. Each nybble represents one out of sixteen combinations of the palette registers 556 in a 4 bit address 553. By setting a bit in the control register 558, either the foreground color or the background color can be selected via a multiplexer 560. The nybbles 552, 562, etc. are fetched in sequence and displayed until the entire graphics screen 552 has been displayed.

While there has been shown and described the preferred embodiments of the invention, it will be evident to those skilled in the art that various modifications may be made thereto without departing from the spirit and scope of the invention as set forth in the appended claims and their equivalents.

WHAT IS CLAIMED IS:

1. A display system for a subscriber terminal of a subscription television system including a subscriber television receiver which displays the programming of the subscription television system, said display system comprising:

a memory having a first graphics screen definition portion for storing graphics data, a second symbol screen definition portion and a third symbol set definition portion, the second and third portions for storing symbol data;

a display processor for generating a first video signal according to said symbol data and said graphics data stored in said memory; and

a display multiplexer for receiving a second video signal from the subscriber terminal, for receiving said first video signal outputted from said display processor, and for selectively outputting a pixel of one of said first video signal and said second video signal for display on the subscriber television receiver.

2. A display system as set forth in claim 1 wherein: said third symbol set definition portion of said memory contains more than one symbol set definition.

3. A display system as set forth in claim 2 wherein: each symbol set definition has a plurality of characters, each defined by an mxn array of pixels, where m and n are integers.

4. A display system as set forth in claim 3 wherein: at least one of the parameters n and m for one symbol set definition is not the same as n and m for at least one other symbol set definition.

5. A display system as set forth in claim 2 wherein: at least one of said character set definitions has a plurality of characters defining a different language from at least one other character set.

6. A display system as set forth in claim 5 wherein: at least one of said character set definition is English.

7. A display system as set forth in claim 5 wherein: at least one of said character set definition is Chinese.

8. A display system as set forth in claim 5 wherein: at least one of said character set definition is Arabic.

9. A display system as set forth in claim 5 wherein: at least one of said character set definition is Japanese.

10. A display system as set forth in claim 1 wherein: said memory is a random access memory.

11. A display system as set forth in claim 10 wherein: said random access memory is a read/write memory.

12. A display system as set forth in claim 1 wherein: said memory includes a pixel mapped graphics portion.

13. A display system for generating a first video signal comprising:

a memory having a first graphics screen definition portion for storing graphics data, a second symbol screen definition portion and a third symbol set definition portion, said second and third portions for storing symbol data;

display generating means for converting said symbol data and said graphics data stored in said memory to pixel data; and

display processing means, responsive to said display generating means, for converting said pixel data to an analog pixel signal; and

display multiplexing means for generating said first video signal by multiplexing between said analog pixel signal and a second video signal on a pixel by pixel basis.

14. The display system according to claim 13, said symbol data including a plurality of character sets, each of said character sets defining a plurality of characters, wherein each of said characters is defined by an m by n array of pixels.

15. The display system according to claim 14, one of said character sets being an English character set.

16. The display system according to claim 14, one of said character sets being a Chinese character set.

17. The display system according to claim 14, one of said character sets being an Arabic character set.

18. The display system according to claim 14, one of said character sets being a Japanese character set.

19. The display system according to claim 13, said display system being a subsystem of a subscriber terminal of a cable television system.

20. The display system according to claim 13 further comprising control processing means for controlling operation of said display generating means.

21. The display system according to claim 13, said display generating means converting one of said symbol data and said graphics data to said pixel data according to priority data.

22. The display system according to claim 13, said display processing means having pixel conversion means for converting said pixel data to said analog pixel signal, and said display multiplexing means having analog multiplexing means, responsive to said display generating means, for multiplexing between said analog pixel signal and said second video signal.

23. The display system according to claim 22, said pixel data including luminance data and chrominance data, and said pixel conversion means including first digital to analog converter means for converting said luminance data to a luminance signal having a representative DC voltage level, second digital to analog converter means for converting said chrominance data to a sinusoidal chrominance signal having a representative color phase, and analog summation circuit means for summing said luminance signal with said chrominance signal to form said analog pixel signal.

24. The display system according to claim 13 further comprising a clock generation circuit means for generating a pixel clock signal having a plurality of cycles, wherein each cycle of said pixel clock signal represents a single pixel.

25. The display system according to claim 24, said clock generation circuit synchronizes said pixel clock signal with a horizontal synchronization pulse of said second video signal.

26. The display system according to claim 25, said clock generation circuit synchronizing said pixel clock signal with said horizontal synchronization pulse of said second video

signal using a synchronization slicer circuit and a phase-lock loop circuit.

27. The display system according to claim 24, said display generating means having:

synchronization circuit means for generating a first horizontal synchronization signal, a vertical synchronization signal, a pixel number signal, and a line number signal in accordance with said pixel clock signal, and for generating a video mode signal that defines a sync tip timing, a color burst timing, a horizontal blanking timing, and a vertical blanking timing in accordance with said first horizontal synchronization signal, said vertical synchronization signal, said pixel number signal, and said line number signal; and

pixel generation circuit means for receiving said video mode signal from said synchronization circuit means and for converting said symbol data and said graphics data to said pixel data according to said video mode signal.

28. The display system according to claim 27 further comprising means for synthesizing a second horizontal synchronization signal synchronized with a horizontal synchronization pulse of said second video signal, wherein said synchronization circuit means synchronizes said first horizontal synchronization signal, said vertical synchronization signal, said pixel number signal, and said line number signal with said second horizontal synchronization signal.

29. The display system according to claim 27, said synchronization circuit means having a pixel counter and a horizontal line counter.

30. The display system according to claim 27, said pixel generation circuit means having means for detecting when said pixel data represents a transparent color and for controlling said video processing means to select said second video signal when said pixel data representing said transparent color is detected.

31. The display system according to claim 27 further comprising a memory interface circuit and address generation

circuit that operate cooperatively to supply said symbol data and graphics data to said pixel generation circuit means.

32. The display system according to claim 20, said display generating means having a control interface circuit means for providing said control processing means access to configuration registers.

33. A method for use in a display system for generating a first video signal, the display system having a memory with a first graphics screen definition portion for storing graphics data, a second symbol screen definition portion and a third symbol set definition portion, the second and third portions for storing symbol data, said method comprising the steps of:

converting one of said symbol data stored in said second and third portions of said memory and said graphics data stored in said first portion of said memory to pixel data;

converting said pixel data to an analog pixel signal; and

generating said first video signal by multiplexing between said analog pixel signal and a second video signal on a pixel by pixel basis.

34. The method for use in a display system according to claim 33, said symbol data including a plurality of character sets, each of said character sets defining a plurality of characters, wherein each of said characters is defined by an m by n array of pixels.

35. The method for use in a display system according to claim 34, one of said character sets being an English character set.

36. The method for use in a display system according to claim 34, one of said character sets being a Chinese character set.

37. The method for use in a display system according to claim 34, one of said character sets being an Arabic character set.

38. The method for use in a display system according to claim 34, one of said character sets being a Japanese character set.

39. The method for use in a display system according to claim 33, said display system being a subsystem of a subscriber terminal of a cable television system.

40. The method for use in a display system according to claim 33, said converting of one of said symbol data and said graphics data to said pixel data is performed according to priority data.

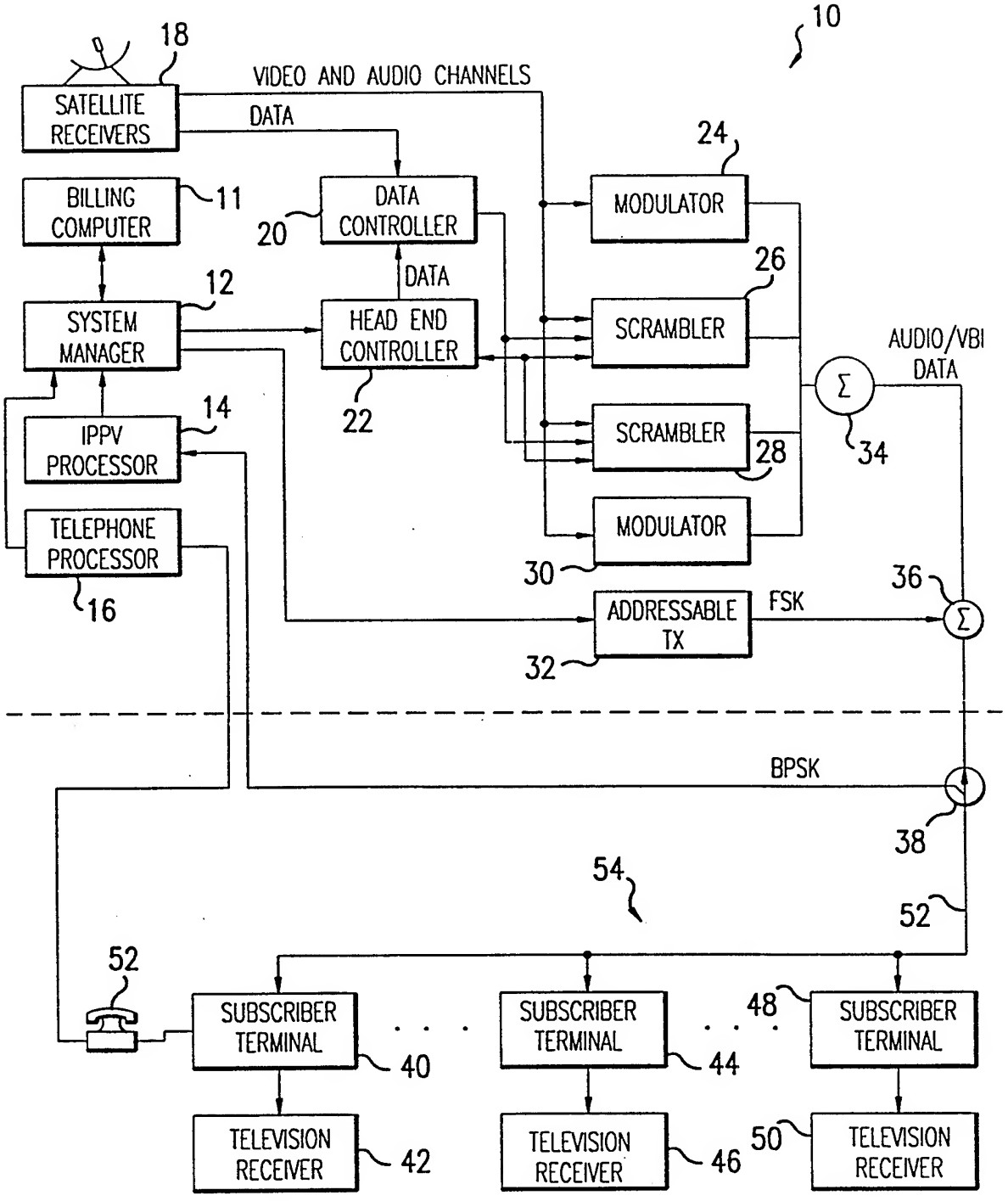
10
18
SATELLITE RECEIVERS
VIDEO AND AUDIO CHANNELS
DATA
24
BILLING COMPUTER
11
20
DATA CONTROLLER
MODULATOR
DATA
26
12
SYSTEM MANAGER
HEAD END CONTROLLER
SCRAMBLER
AUDIO/VBI DATA
Σ
34
22
14
IPPV PROCESSOR
SCRAMBLER
28
MODULATOR
TELEPHONE PROCESSOR
16
30
36
ADDRESSABLE TX
FSK
32
BPSK
38
54
52
52
SUBSCRIBER TERMINAL
40
SUBSCRIBER TERMINAL
44
48
SUBSCRIBER TERMINAL
TELEVISION RECEIVER
42
TELEVISION RECEIVER
46
50
TELEVISION RECEIVER

FIG.1

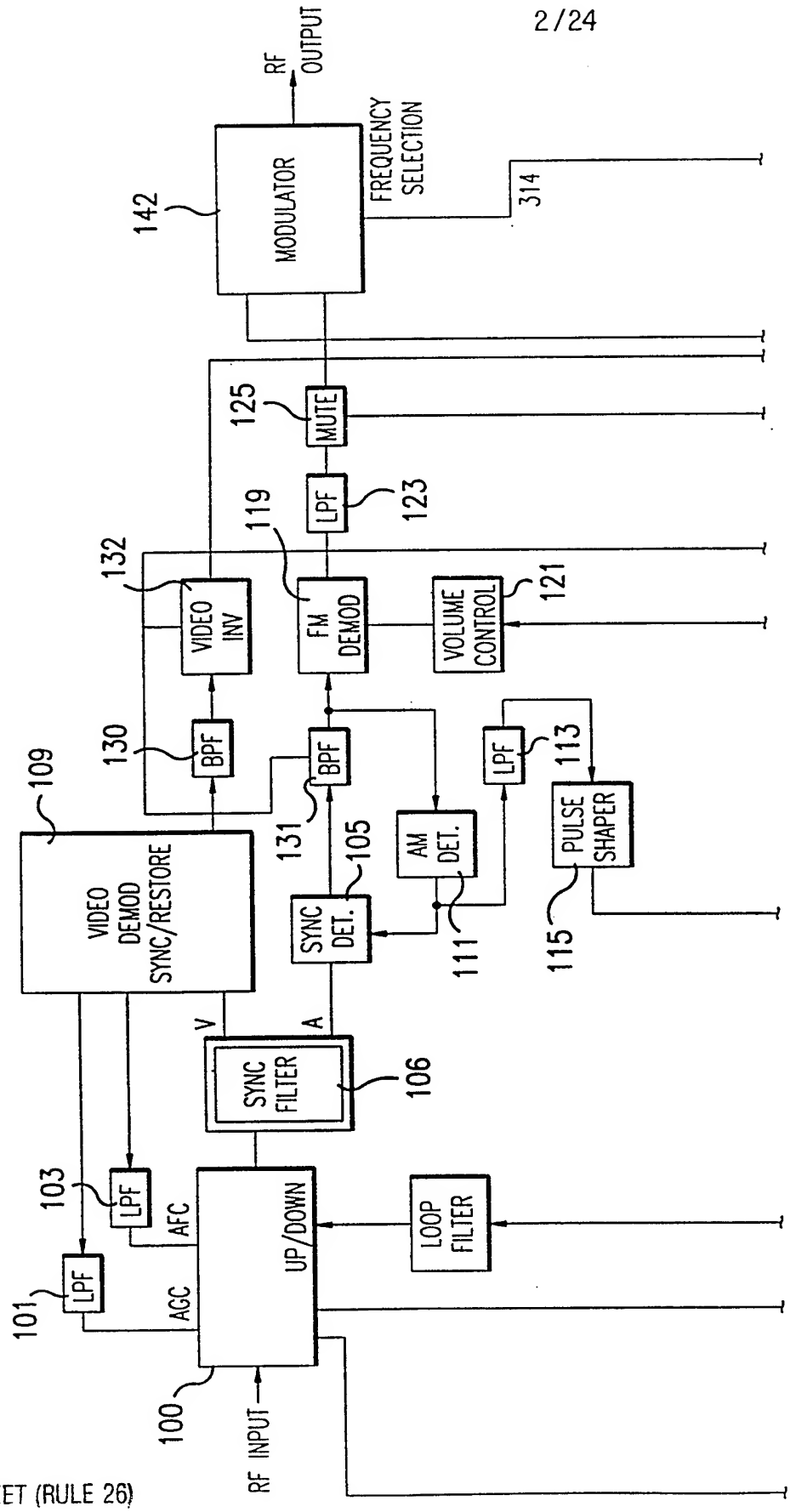
RF OUTPUT
142
MODULATOR
FREQUENCY SELECTION
314
125
MUTE
LPF
123
119
132
VIDEO INV
FM DEMOD
VOLUME CONTROL
121
130
BPF
BPF
131
109
VIDEO DEMOD SYNC/RESTORE
105
AM DET.
LPF
113
PULSE SHAPER
SYNC DET.
111
115
V
A
SYNC FILTER
106
103
LPF
AFC
UP/DOWN
LOOP FILTER
101
LPF
AGC
100
RF INPUT

FIG.2A

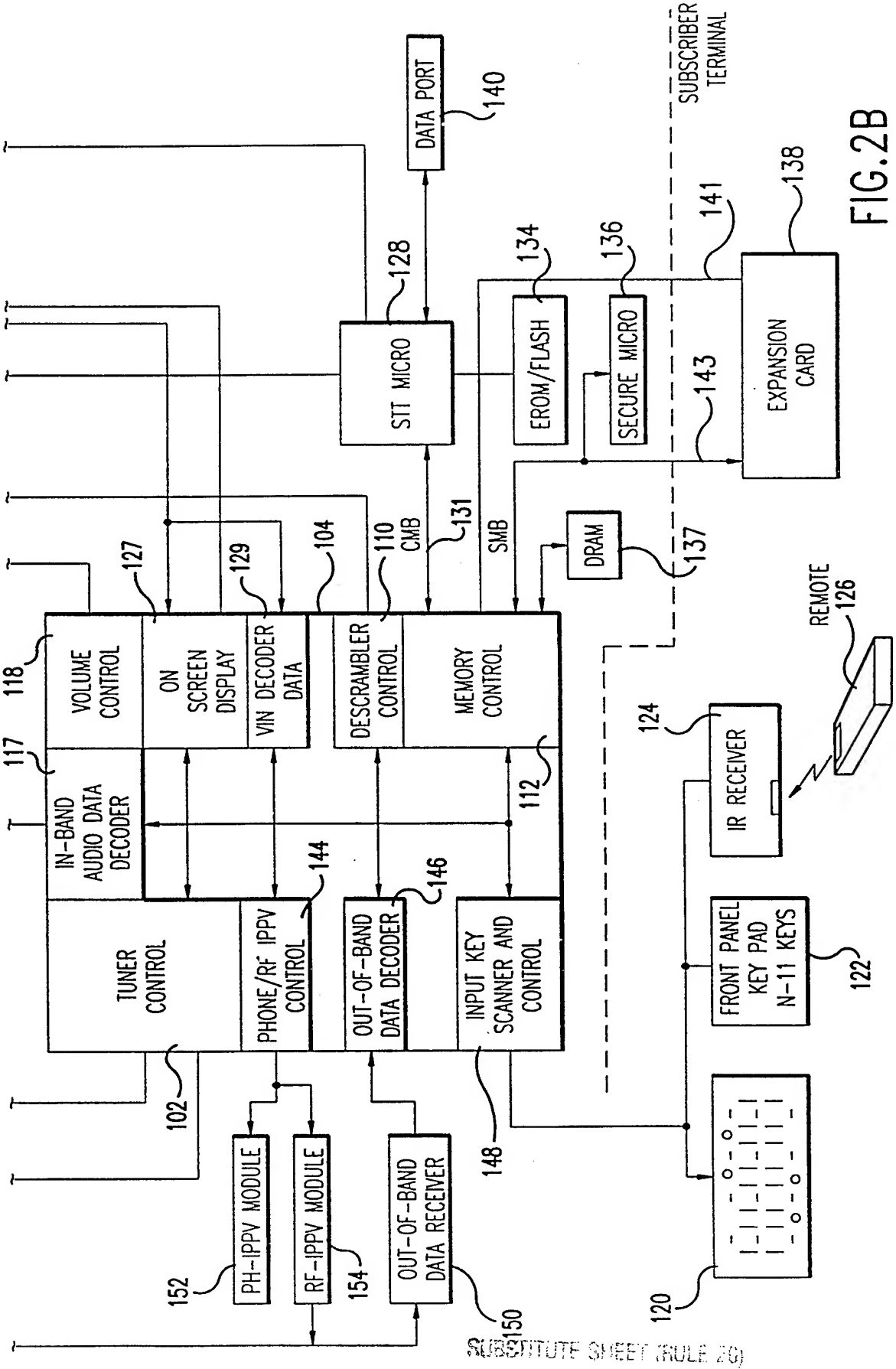
SUBSCRIBER TERMINAL
DATA PORT
140
STT MICRO
128
EROM/FLASH
134
SECURE MICRO
136
141
EXPANSION CARD
138
143
DRAM
137
131
CMB
SMB
110
104
129
127
118
VOLUME CONTROL
ON SCREEN DISPLAY
VIN DECODER DATA
DESCRAMBLER CONTROL
MEMORY CONTROL
117
IN-BAND AUDIO DATA DECODER
112
124
IR RECEIVER
REMOTE
126
144
146
TUNER CONTROL
PHONE/RF IPPV CONTROL
OUT-OF-BAND DATA DECODER
INPUT KEY SCANNER AND CONTROL
FRONT PANEL KEY PAD N-11 KEYS
122
102
148
PH-IPPV MODULE
RF-IPPV MODULE
OUT-OF-BAND DATA RECEIVER
152
154
150
120

FIG.2B

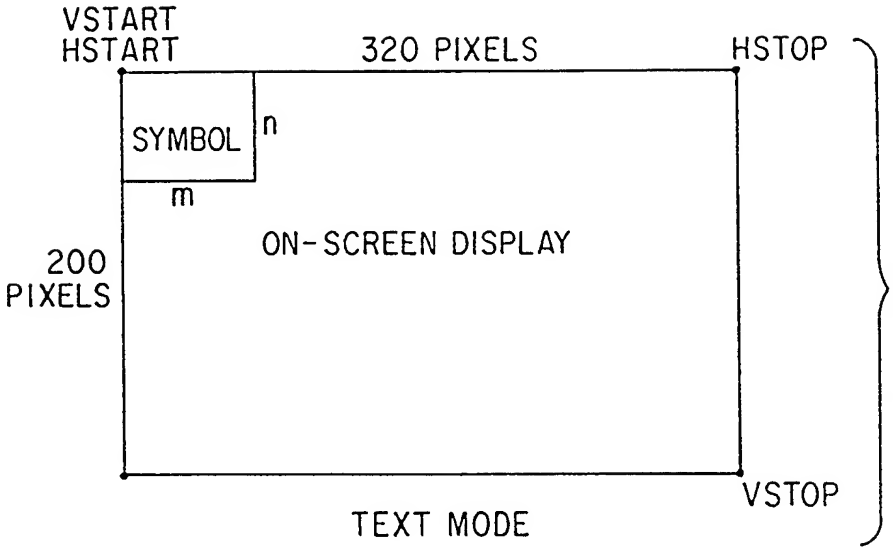

FIG. 3

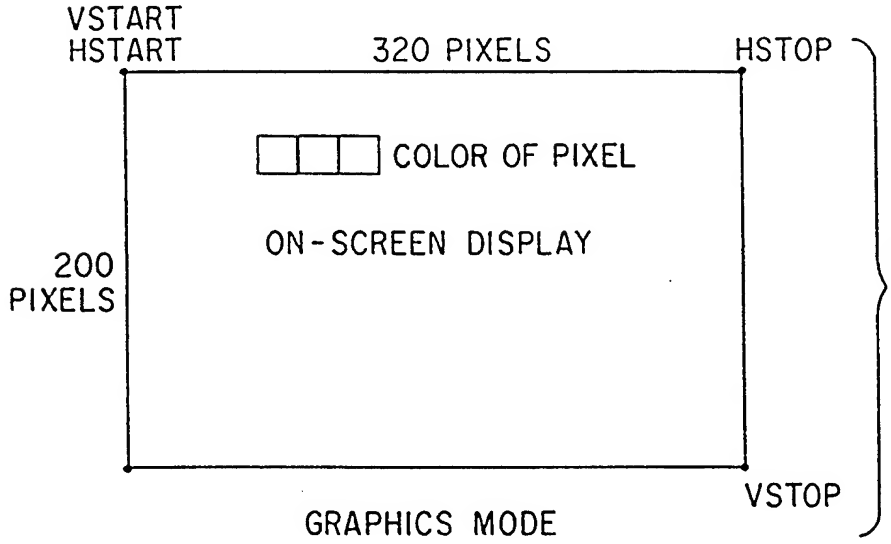

FIG. 4

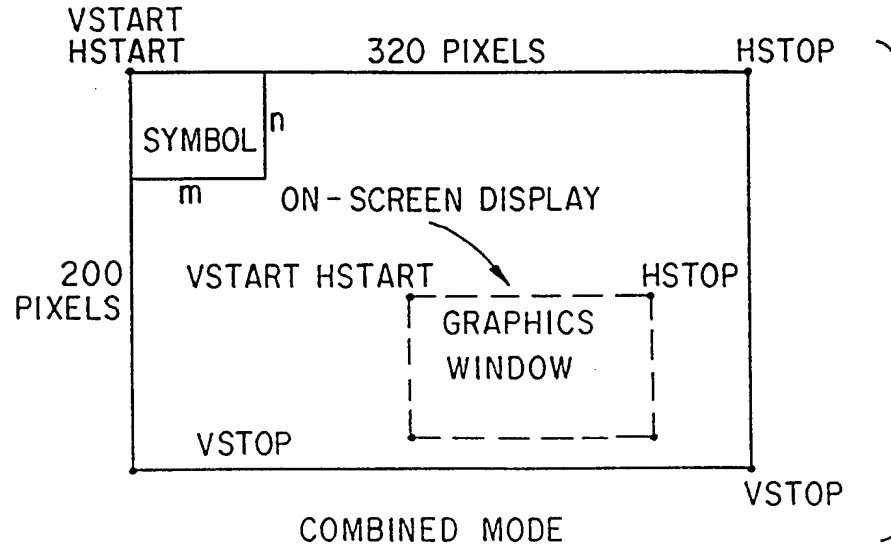

FIG. 5

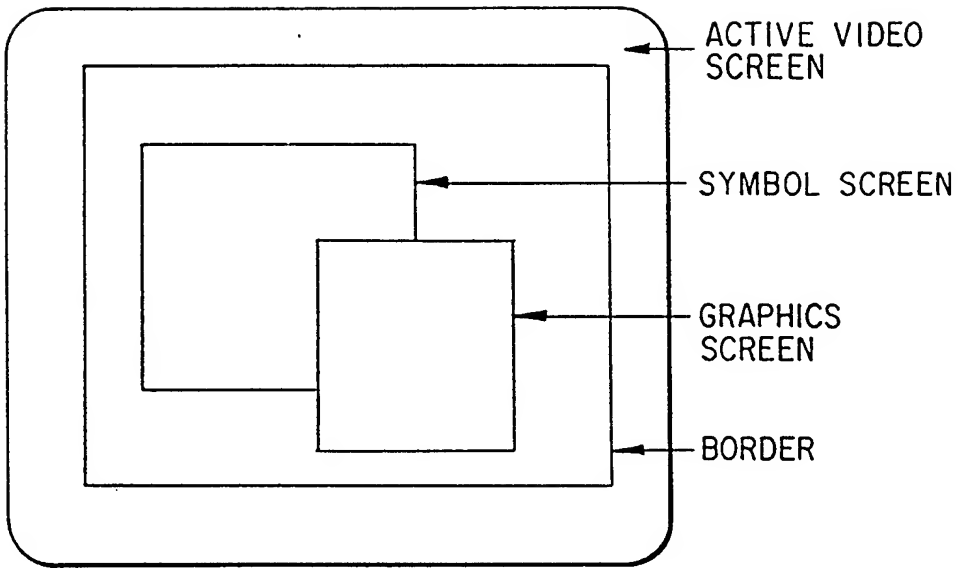

FIG. 6

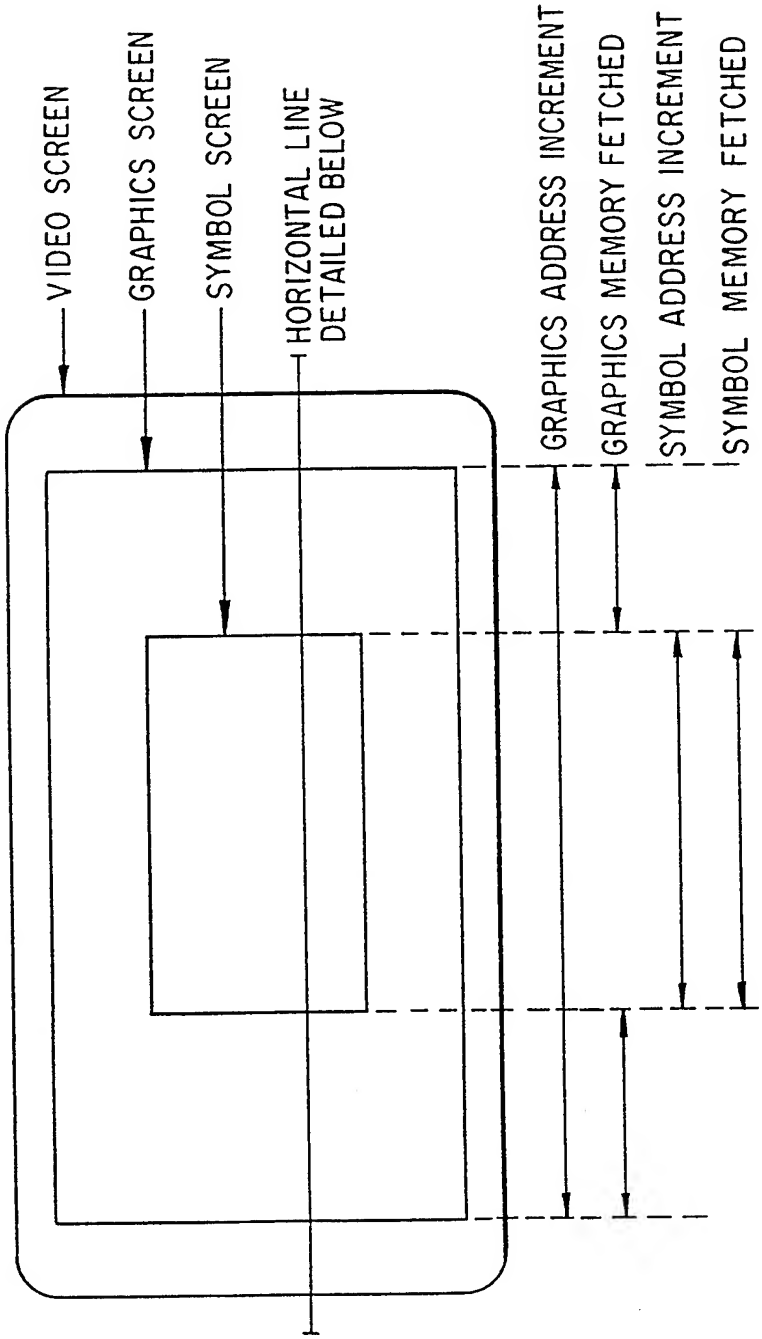
VIDEO SCREEN
GRAPHICS SCREEN
SYMBOL SCREEN
HORIZONTAL LINE DETAILED BELOW
GRAPHICS ADDRESS INCREMENT
GRAPHICS MEMORY FETCHED
SYMBOL ADDRESS INCREMENT
SYMBOL MEMORY FETCHED

FIG. 7

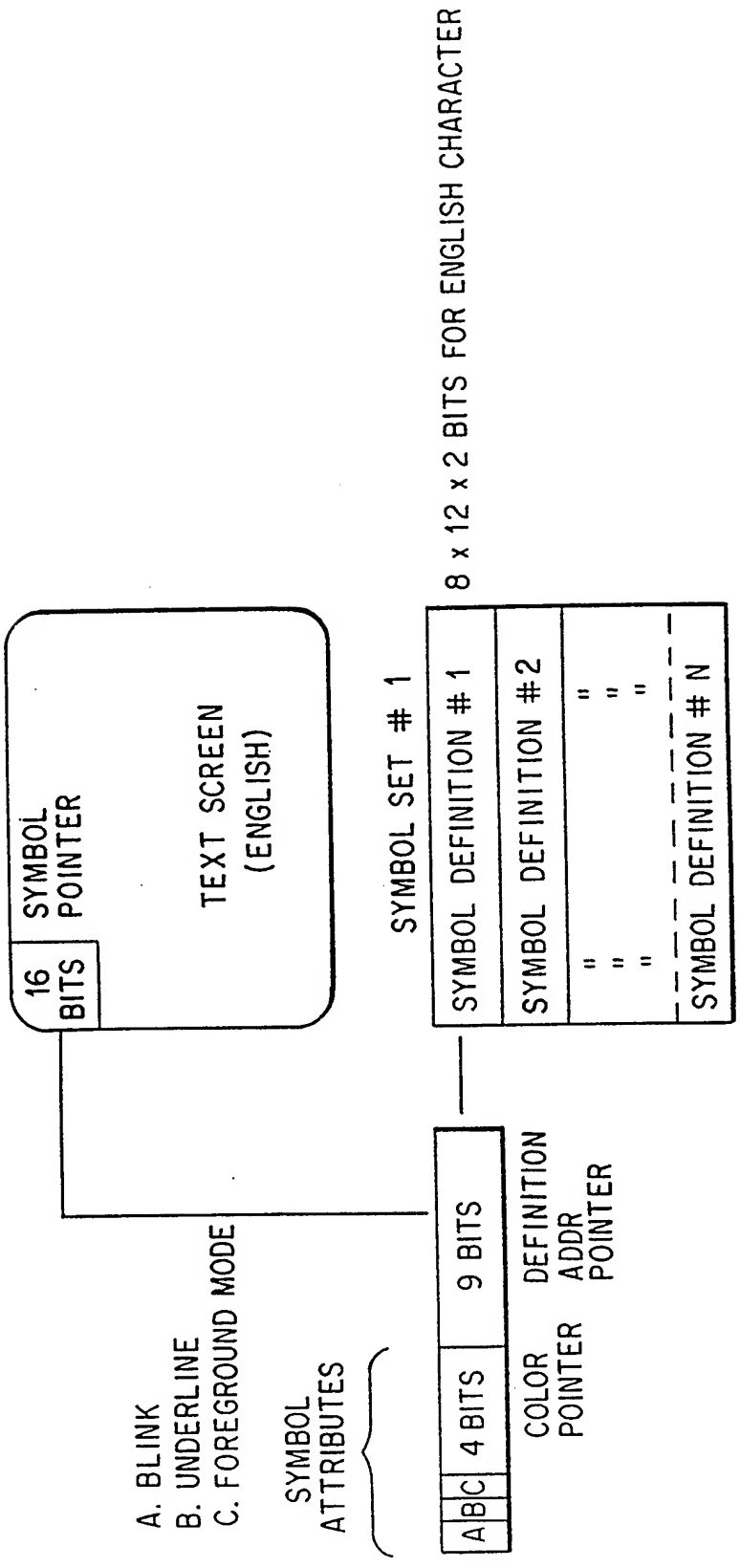
8 x 12 x 2 BITS FOR ENGLISH CHARACTER
SYMBOL SET # 1
SYMBOL DEFINITION # 1
SYMBOL DEFINITION #2
SYMBOL DEFINITION # N
16 BITS
SYMBOL POINTER
TEXT SCREEN (ENGLISH)
A. BLINK
B. UNDERLINE
C. FOREGROUND MODE
SYMBOL ATTRIBUTES
A B C
4 BITS
9 BITS
COLOR POINTER
DEFINITION ADDR POINTER

FIG. 8

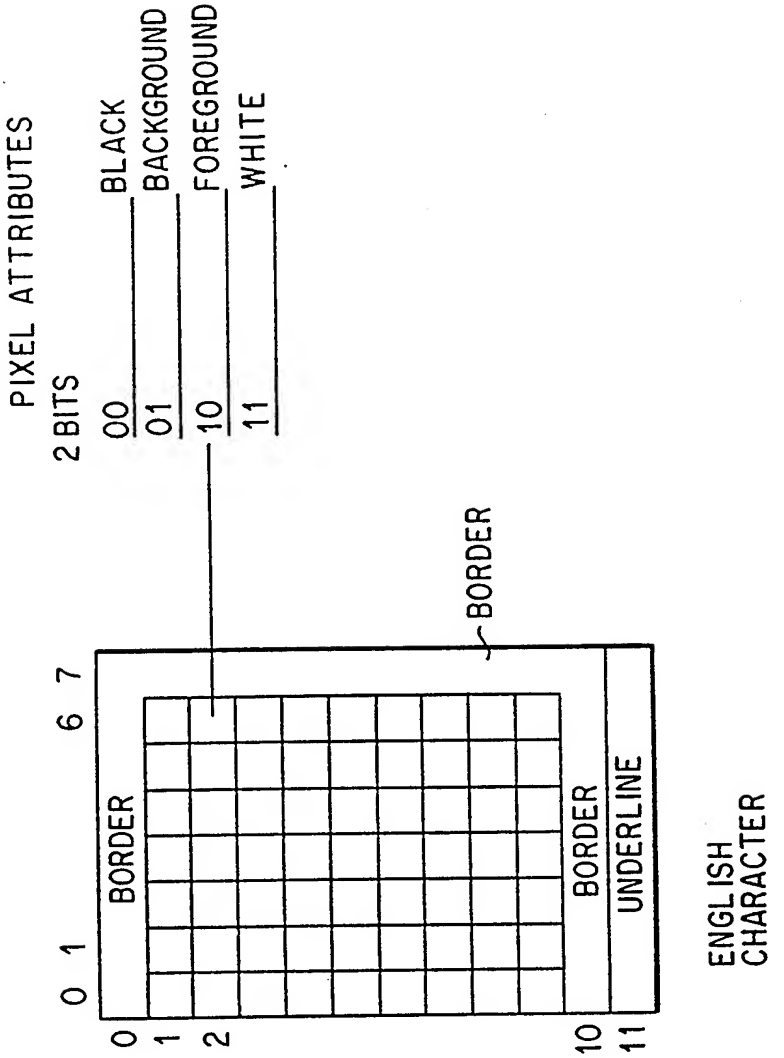
PIXEL ATTRIBUTES
2 BITS
00 BLACK
01 BACKGROUND
10 FOREGROUND
11 WHITE
BORDER
0 1
6 7
BORDER
BORDER
UNDERLINE
0
1
2
10
11
ENGLISH CHARACTER

FIG. 9

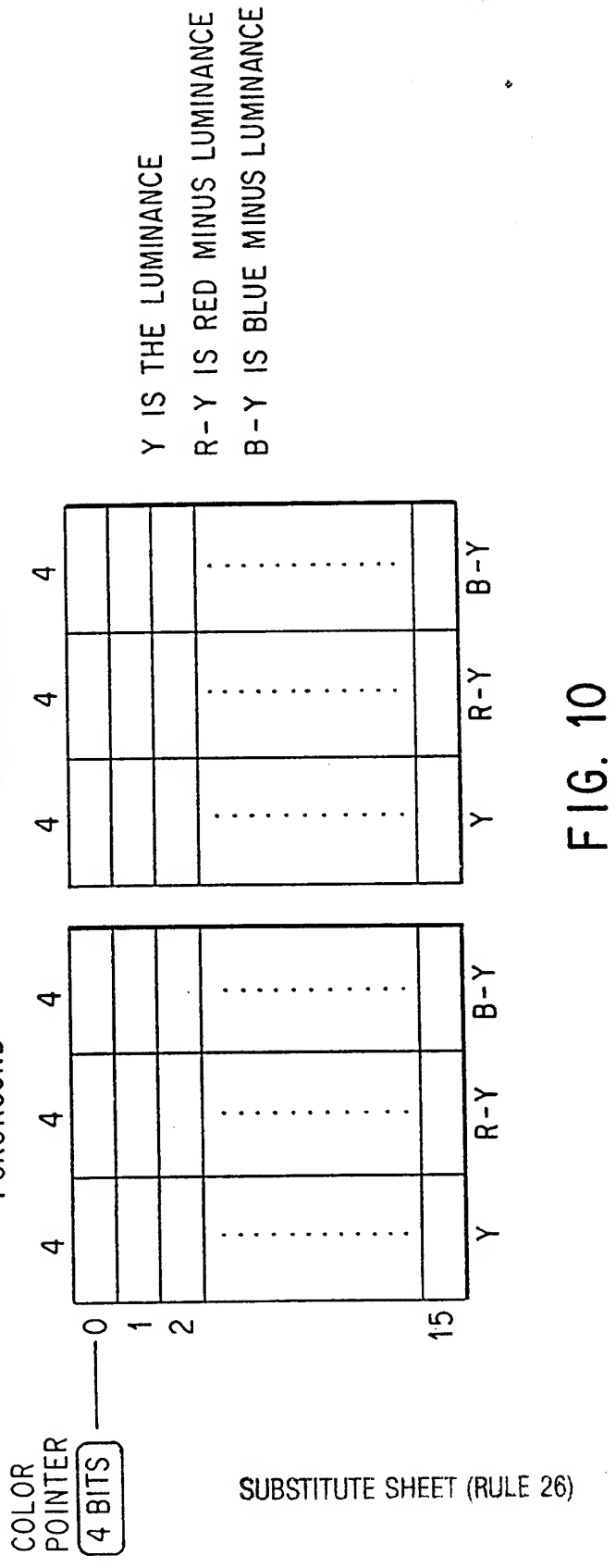
Y IS THE LUMINANCE
R-Y IS RED MINUS LUMINANCE
B-Y IS BLUE MINUS LUMINANCE
PALETTE REGISTERS
BACKGROUND
FORGROUND
4
4
4
Y
R-Y
B-Y
COLOR POINTER
4 BITS
0
1
2
15

FIG. 10

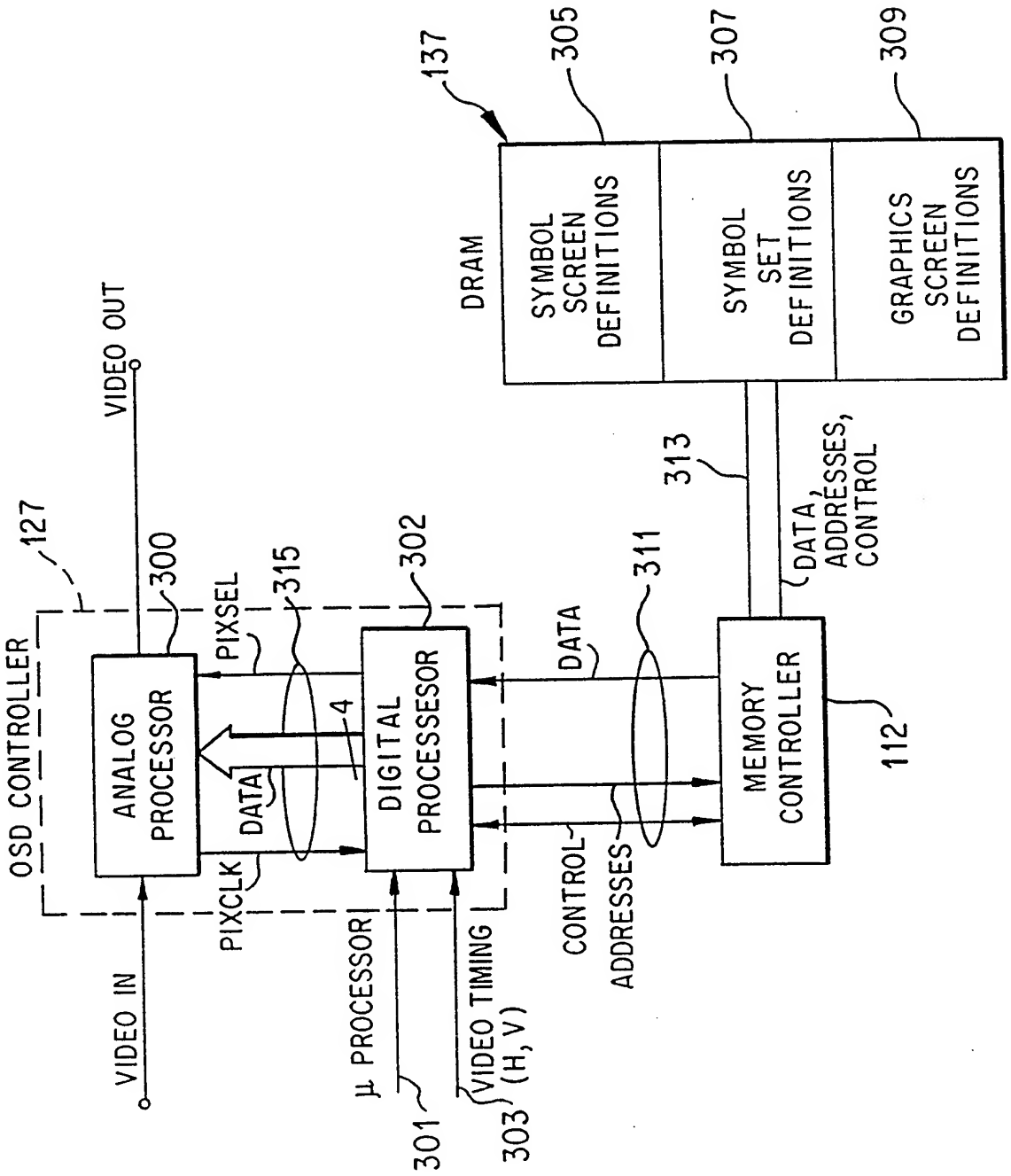
137
305
307
309
DRAM
SYMBOL SCREEN DEFINITIONS
SYMBOL SET DEFINITIONS
GRAPHICS SCREEN DEFINITIONS
313
DATA, ADDRESSES, CONTROL
VIDEO OUT
127
300
315
302
311
OSD CONTROLLER
ANALOG PROCESSOR
PIXSEL
4
DATA
DIGITAL PROCESSESOR
DATA
MEMORY CONTROLLER
112
PIXCLK
CONTROL
ADDRESSES
VIDEO IN
µ PROCESSOR
VIDEO TIMING (H, V)
301
303

FIG. 11

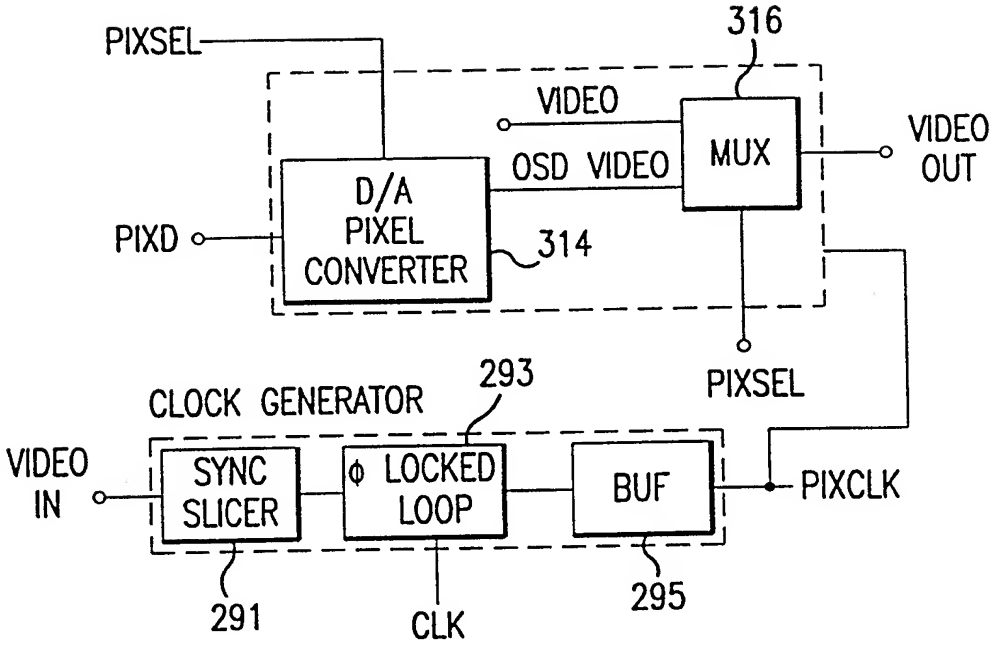
PIXSEL
316
VIDEO
OSD VIDEO
MUX
VIDEO OUT
D/A PIXEL CONVERTER
314
PIXD
PIXSEL
293
CLOCK GENERATOR
VIDEO IN
SYNC SLICER
φ LOCKED LOOP
BUF
PIXCLK
291
CLK
295

FIG.12

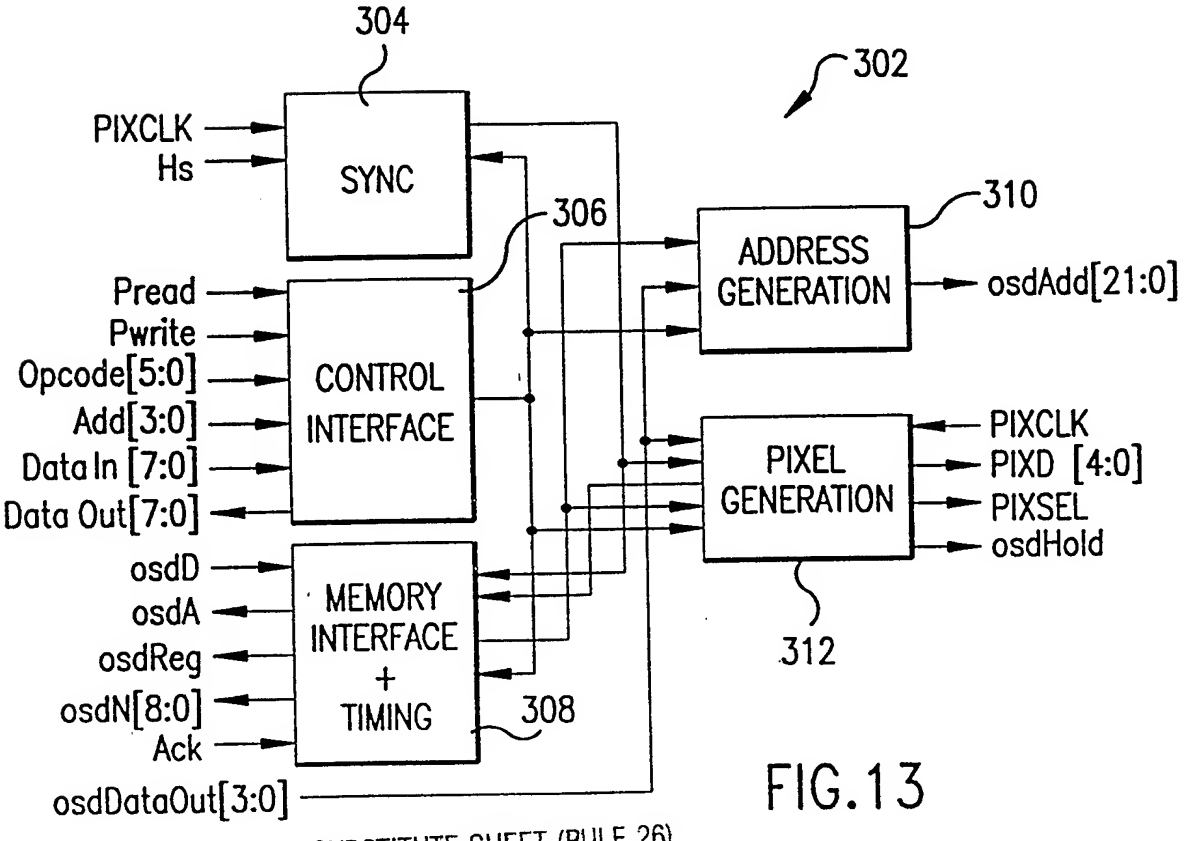
304
302
PIXCLK
Hs
SYNC
306
310
ADDRESS GENERATION
osdAdd[21:0]
Pread
Pwrite
Opcode[5:0]
Add[3:0]
Data In [7:0]
Data Out[7:0]
CONTROL INTERFACE
PIXEL GENERATION
PIXCLK
PIXD [4:0]
PIXSEL
osdHold
312
osdD
osdA
osdReg
osdN[8:0]
Ack
MEMORY INTERFACE + TIMING
308
osdDataOut[3:0]

FIG.13

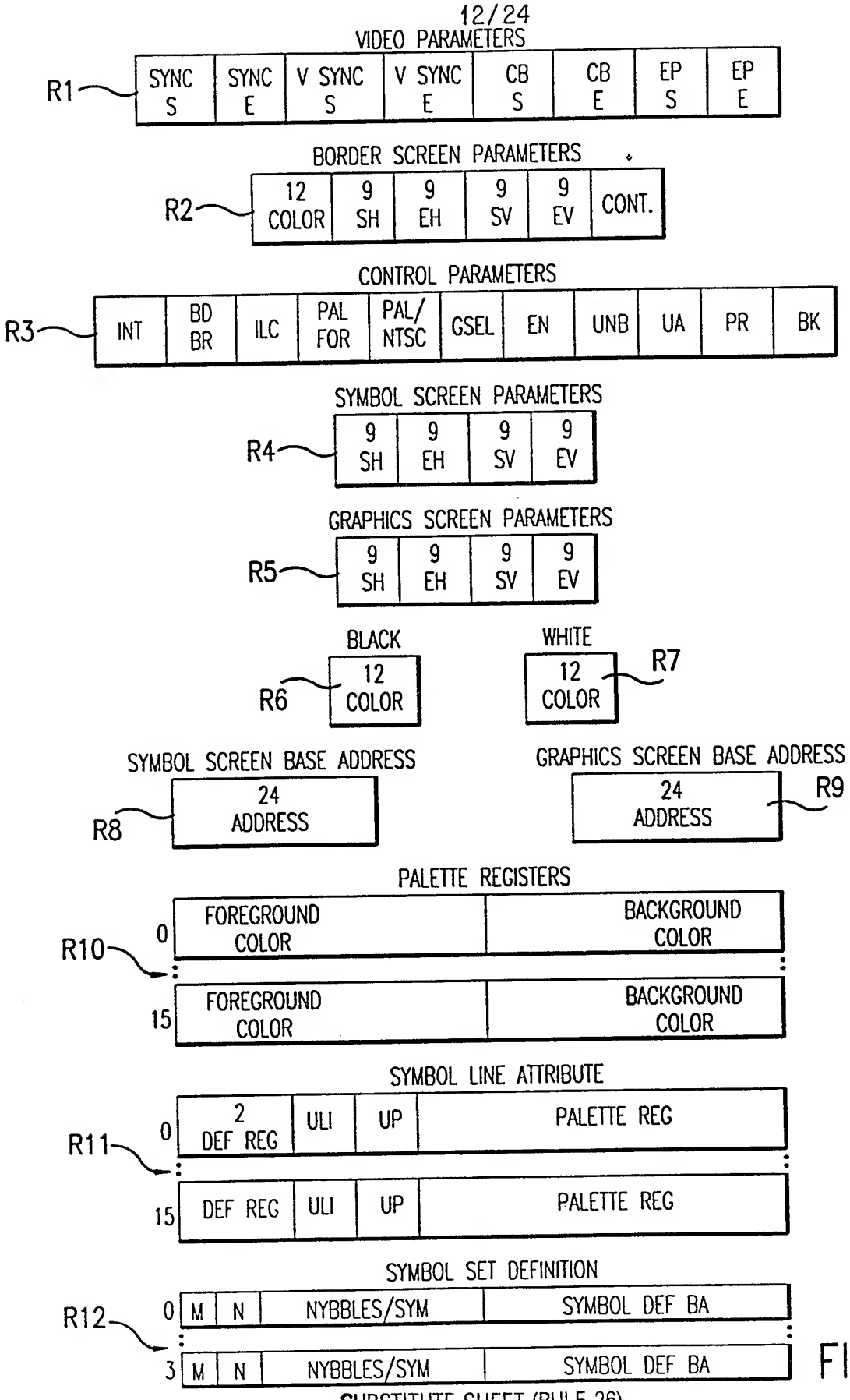
VIDEO PARAMETERS
R1
SYNC S
SYNC E
V SYNC S
V SYNC E
CB S
CB E
EP S
EP E
BORDER SCREEN PARAMETERS
R2
12 COLOR
9 SH
9 EH
9 SV
9 EV
CONT.
CONTROL PARAMETERS
R3
INT
BD BR
ILC
PAL FOR
PAL/ NTSC
GSEL
EN
UNB
UA
PR
BK
SYMBOL SCREEN PARAMETERS
R4
9 SH
9 EH
9 SV
9 EV
GRAPHICS SCREEN PARAMETERS
R5
9 SH
9 EH
9 SV
9 EV
BLACK
R6
12 COLOR
WHITE
12 COLOR
R7
SYMBOL SCREEN BASE ADDRESS
R8
24 ADDRESS
GRAPHICS SCREEN BASE ADDRESS
24 ADDRESS
R9
PALETTE REGISTERS
R10
0
FOREGROUND COLOR
BACKGROUND COLOR
15
FOREGROUND COLOR
BACKGROUND COLOR
SYMBOL LINE ATTRIBUTE
R11
0
2 DEF REG
ULI
UP
PALETTE REG
15
DEF REG
ULI
UP
PALETTE REG
SYMBOL SET DEFINITION
R12
0
M
N
NYBBLES/SYM
SYMBOL DEF BA
3
M
N
NYBBLES/SYM
SYMBOL DEF BA

FIG.14

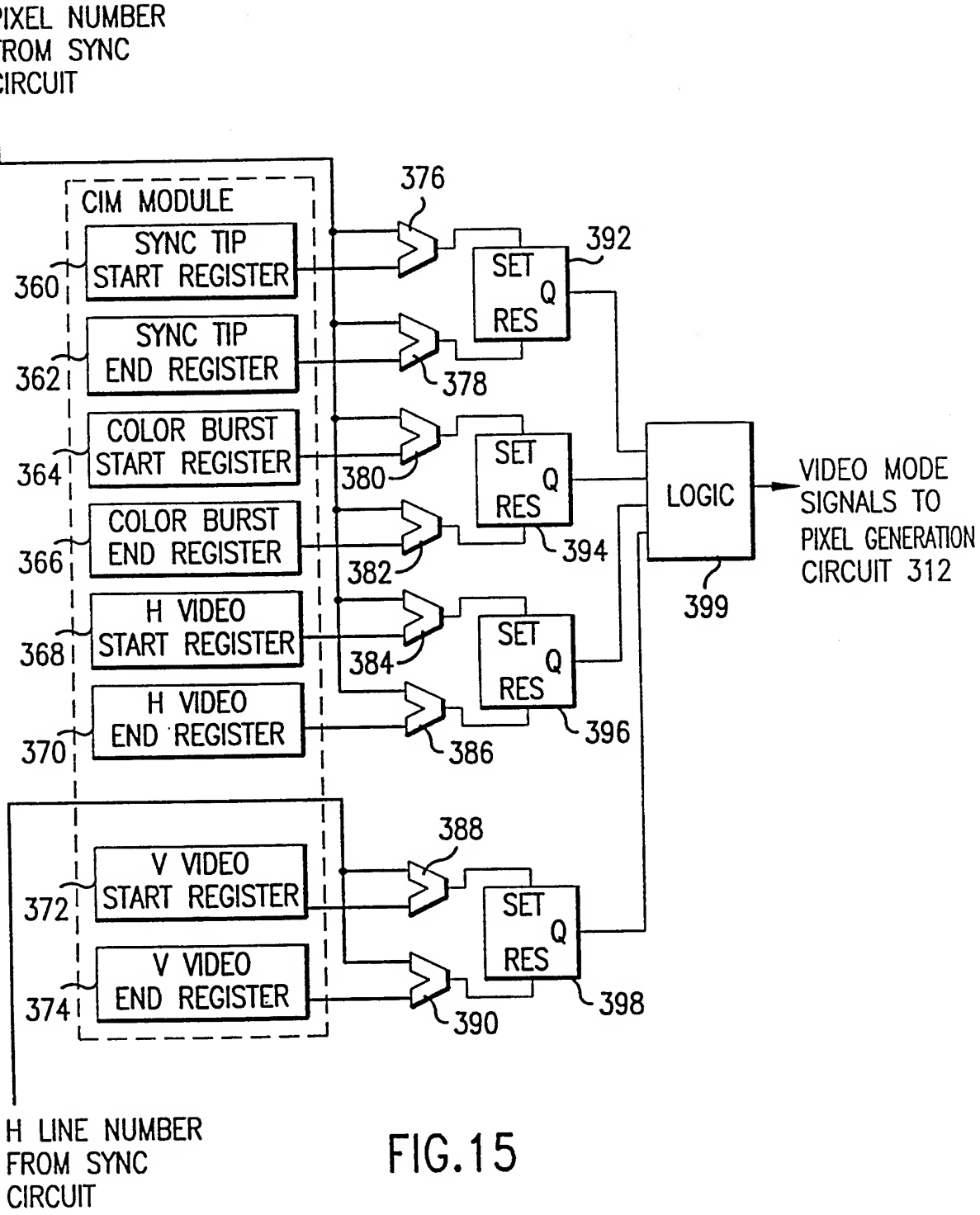
PIXEL NUMBER FROM SYNC CIRCUIT
CIM MODULE
SYNC TIP START REGISTER
360
SYNC TIP END REGISTER
362
COLOR BURST START REGISTER
364
COLOR BURST END REGISTER
366
H VIDEO START REGISTER
368
H VIDEO END REGISTER
370
V VIDEO START REGISTER
372
V VIDEO END REGISTER
374
376
378
380
382
384
386
388
390
SET Q RES
392
394
396
398
LOGIC
399
VIDEO MODE SIGNALS TO PIXEL GENERATION CIRCUIT 312
H LINE NUMBER FROM SYNC CIRCUIT

FIG.15

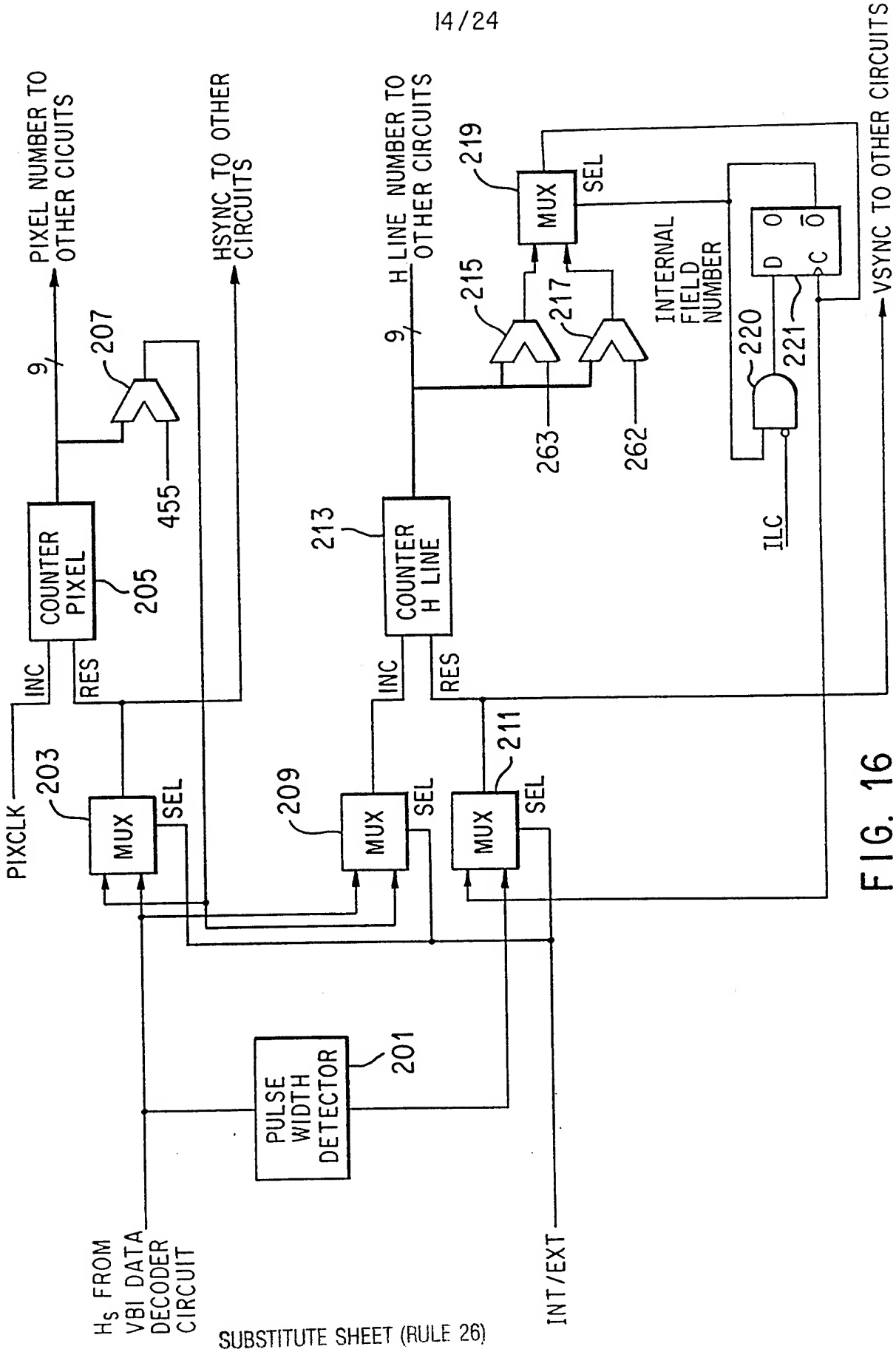
PIXEL NUMBER TO OTHER CICUITS
HSYNC TO OTHER CIRCUITS
H LINE NUMBER TO OTHER CIRCUITS
VSYNC TO OTHER CIRCUITS
INTERNAL FIELD NUMBER
COUNTER PIXEL
205
COUNTER H LINE
213
MUX
SEL
203
209
211
219
215
217
207
455
263
262
220
221
ILC
INC
RES
PIXCLK
PULSE WIDTH DETECTOR
201
H_S FROM VBI DATA DECODER CIRCUIT
INT/EXT

FIG. 16

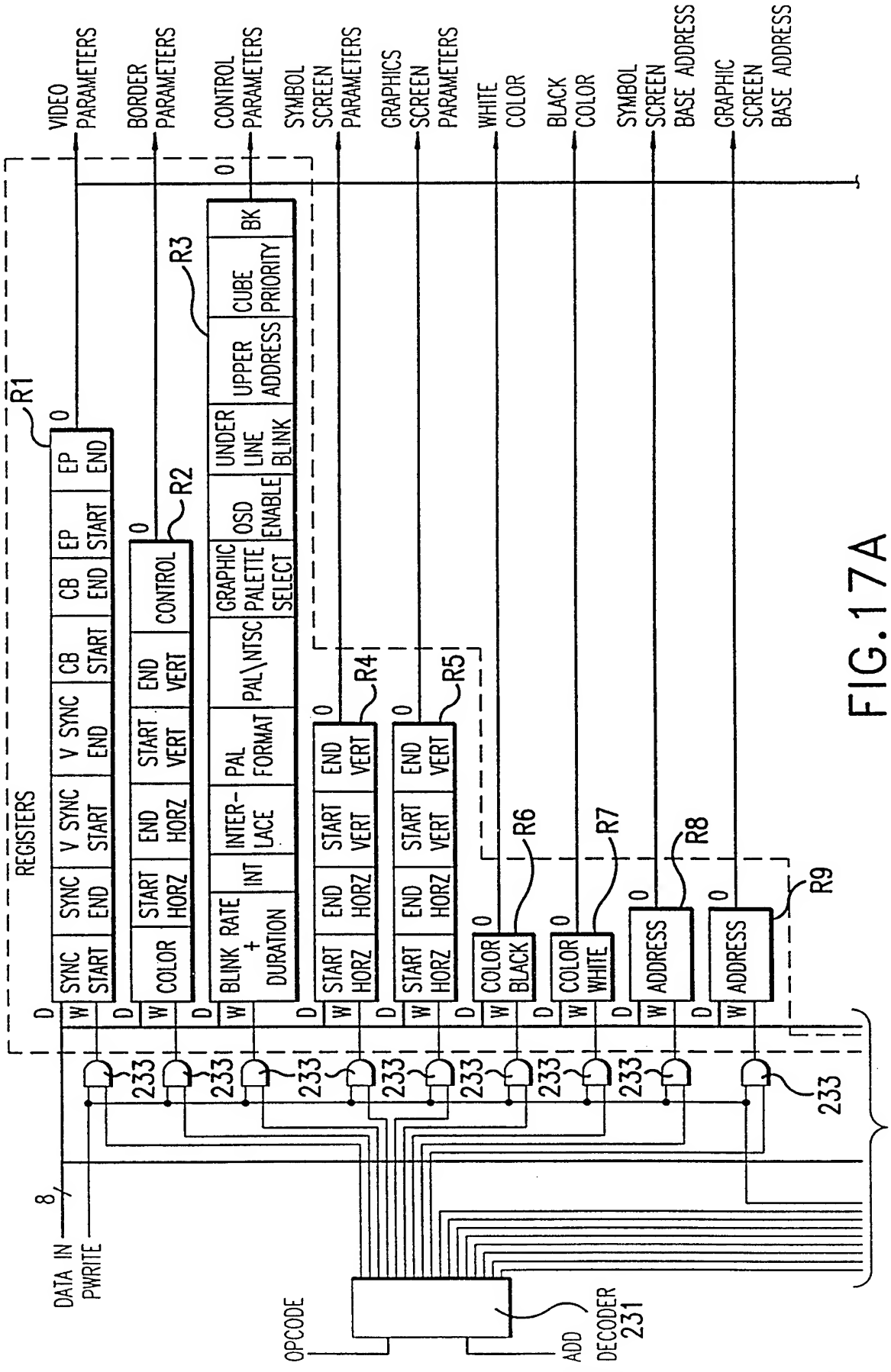
VIDEO PARAMETERS
BORDER PARAMETERS
CONTROL PARAMETERS
SYMBOL SCREEN PARAMETERS
GRAPHICS SCREEN PARAMETERS
WHITE COLOR
BLACK COLOR
SYMBOL SCREEN BASE ADDRESS
GRAPHIC SCREEN BASE ADDRESS
REGISTERS
R1
R2
R3
R4
R5
R6
R7
R8
R9
SYNC START
SYNC END
V SYNC START
V SYNC END
CB START
CB END
EP START
EP END
COLOR
START HORZ
END HORZ
INTER-LACE
PAL FORMAT
START VERT
END VERT
PAL\NTSC
CONTROL
BLINK RATE + DURATION
GRAPHIC PALETTE SELECT
OSD ENABLE
UNDER LINE BLINK
UPPER ADDRESS
CUBE PRIORITY
BK
COLOR BLACK
COLOR WHITE
ADDRESS
233
8
DATA IN
PWRITE
OPCODE
ADD
DECODER 231

FIG.17A

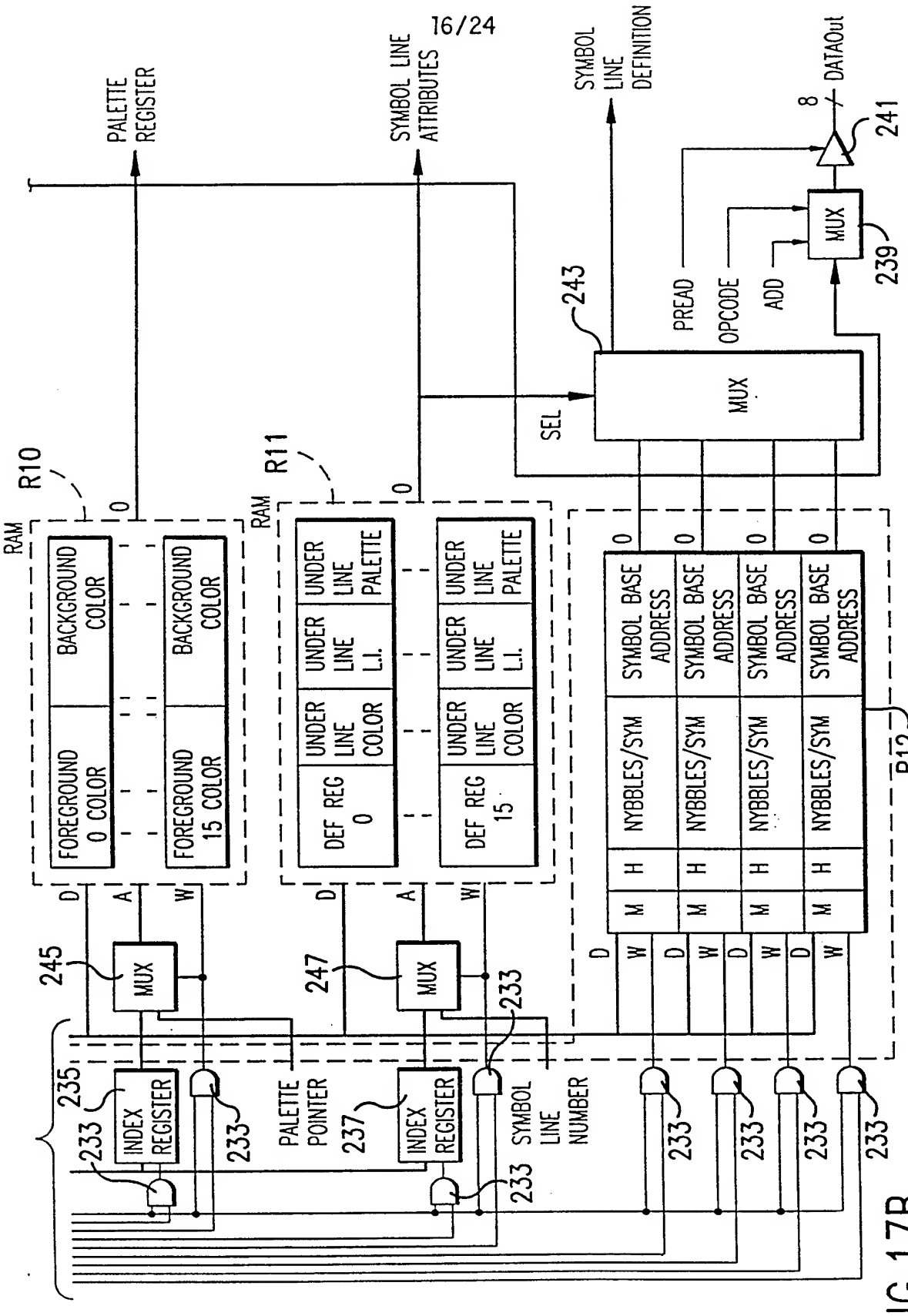
PALETTE REGISTER
SYMBOL LINE ATTRIBUTES
SYMBOL LINE DEFINITION
DATAOut
8
241
PREAD
OPCODE
ADD
MUX
239
243
SEL
MUX
R10
R11
R12
RAM
RAM
FOREGROUND 0 COLOR
BACKGROUND COLOR
FOREGROUND 15 COLOR
BACKGROUND COLOR
DEF REG 0
UNDER LINE COLOR
UNDER LINE L.I.
UNDER LINE PALETTE
DEF REG 15
UNDER LINE COLOR
UNDER LINE L.I.
UNDER LINE PALETTE
M
H
NYBBLES/SYM
SYMBOL BASE ADDRESS
D
W
A
245
247
MUX
MUX
233
235
INDEX REGISTER
PALETTE POINTER
237
INDEX REGISTER
SYMBOL LINE NUMBER

FIG.17B

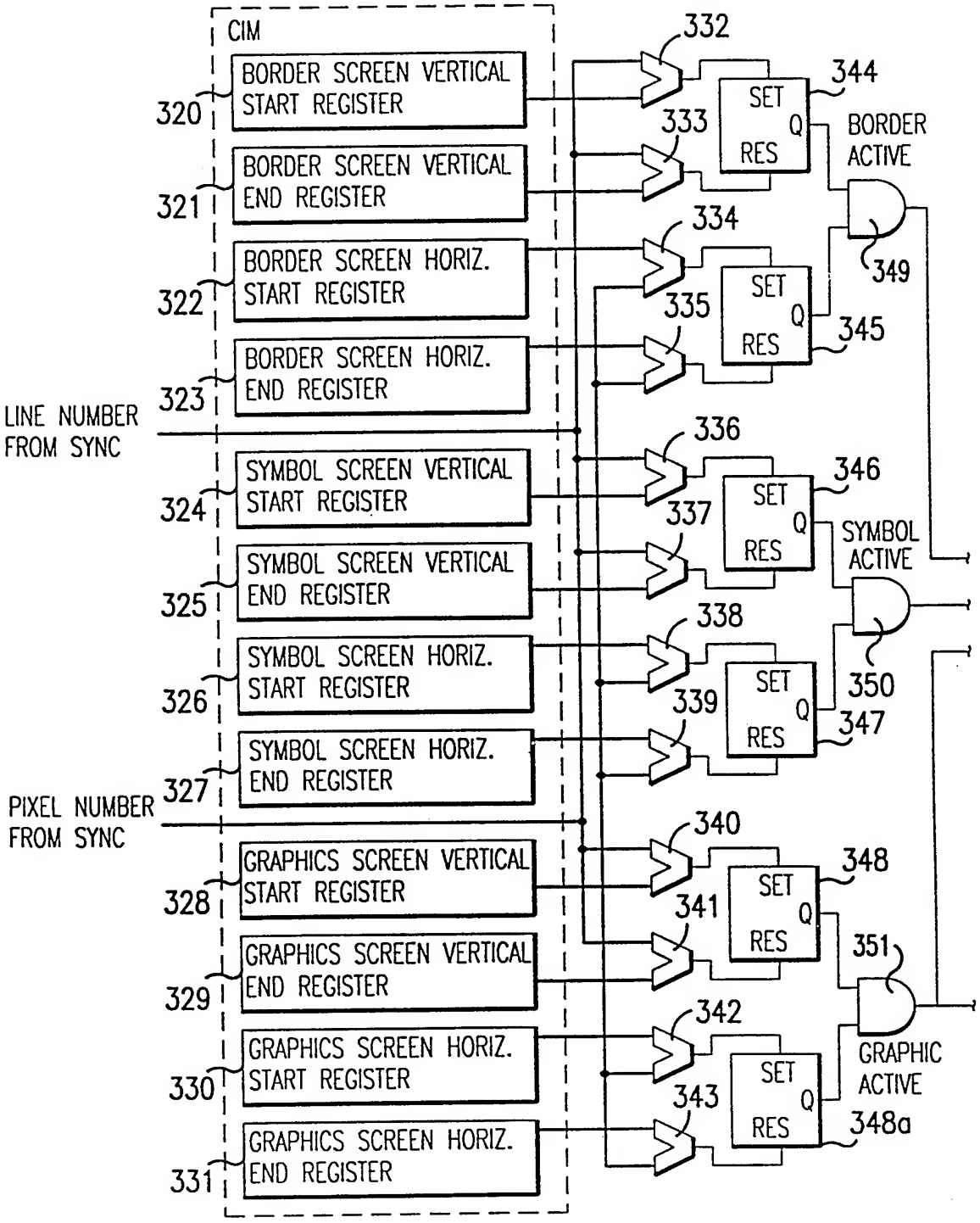
CIM
BORDER SCREEN VERTICAL START REGISTER
320
BORDER SCREEN VERTICAL END REGISTER
321
BORDER SCREEN HORIZ. START REGISTER
322
BORDER SCREEN HORIZ. END REGISTER
323
LINE NUMBER FROM SYNC
SYMBOL SCREEN VERTICAL START REGISTER
324
SYMBOL SCREEN VERTICAL END REGISTER
325
SYMBOL SCREEN HORIZ. START REGISTER
326
SYMBOL SCREEN HORIZ. END REGISTER
327
PIXEL NUMBER FROM SYNC
GRAPHICS SCREEN VERTICAL START REGISTER
328
GRAPHICS SCREEN VERTICAL END REGISTER
329
GRAPHICS SCREEN HORIZ. START REGISTER
330
GRAPHICS SCREEN HORIZ. END REGISTER
331
332
333
334
335
336
337
338
339
340
341
342
343
SET
RES
Q
344
345
346
347
348
348a
BORDER ACTIVE
349
SYMBOL ACTIVE
350
351
GRAPHIC ACTIVE

FIG.18A

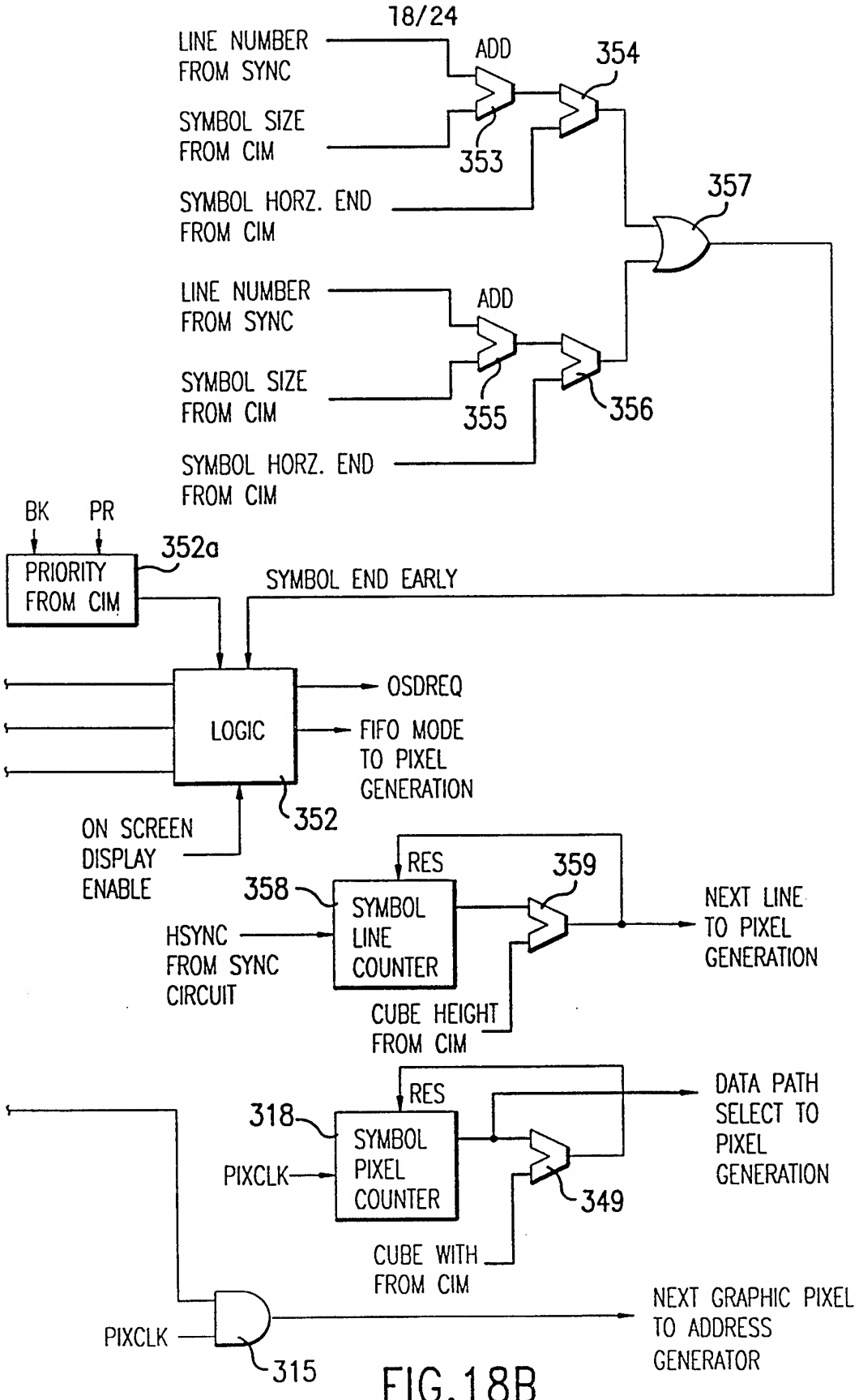
LINE NUMBER FROM SYNC
ADD
354
SYMBOL SIZE FROM CIM
353
SYMBOL HORZ. END FROM CIM
357
LINE NUMBER FROM SYNC
ADD
SYMBOL SIZE FROM CIM
355
356
SYMBOL HORZ. END FROM CIM
BK
PR
352a
PRIORITY FROM CIM
SYMBOL END EARLY
LOGIC
OSDREQ
FIFO MODE TO PIXEL GENERATION
352
ON SCREEN DISPLAY ENABLE
RES
359
358
SYMBOL LINE COUNTER
HSYNC FROM SYNC CIRCUIT
NEXT LINE TO PIXEL GENERATION
CUBE HEIGHT FROM CIM
RES
318
SYMBOL PIXEL COUNTER
PIXCLK
DATA PATH SELECT TO PIXEL GENERATION
349
CUBE WITH FROM CIM
PIXCLK
NEXT GRAPHIC PIXEL TO ADDRESS GENERATOR
315

FIG.18B

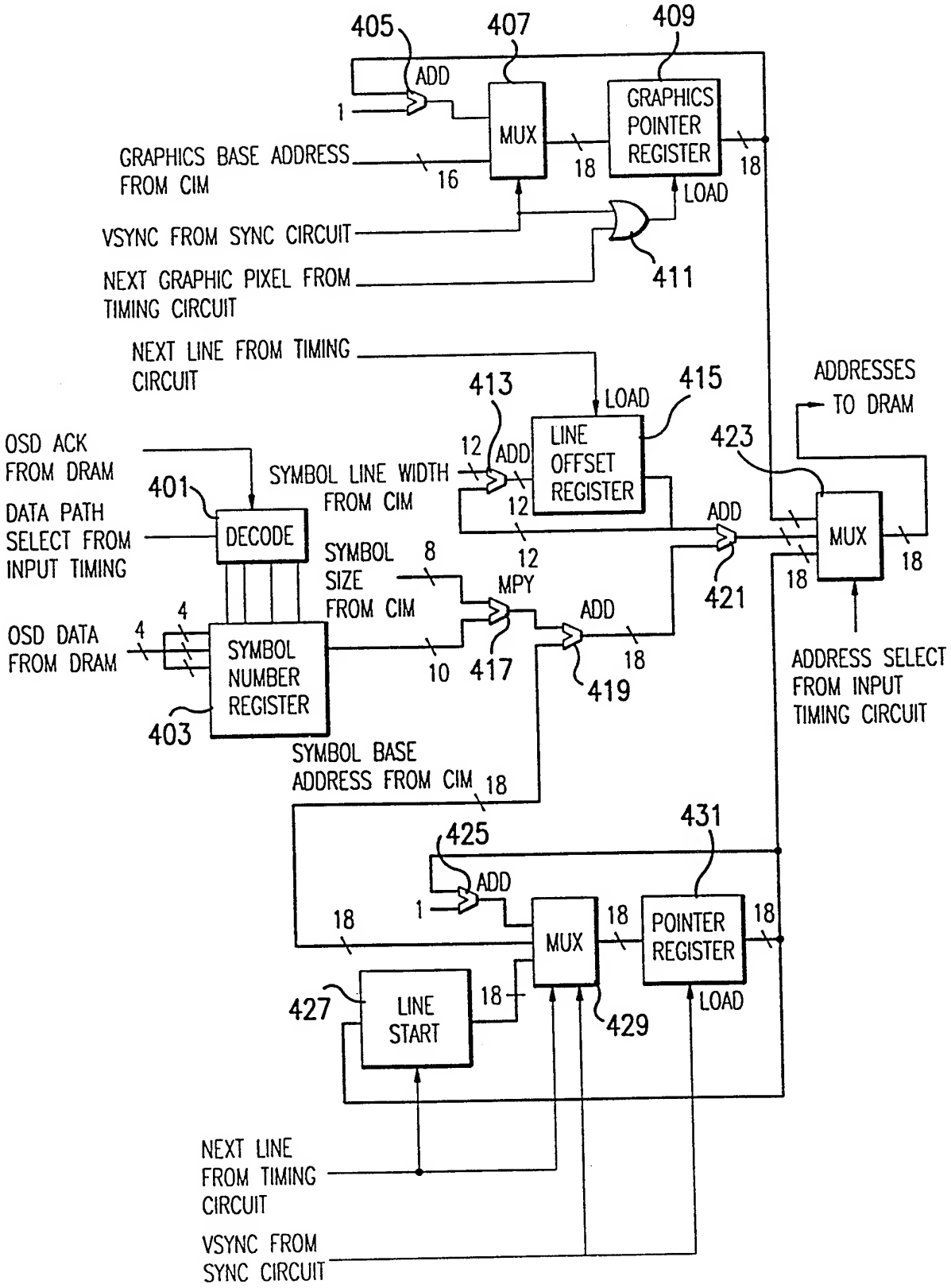
405
407
409
ADD
1
MUX
GRAPHICS POINTER REGISTER
GRAPHICS BASE ADDRESS FROM CIM
16
18
18
LOAD
VSYNC FROM SYNC CIRCUIT
NEXT GRAPHIC PIXEL FROM TIMING CIRCUIT
411
NEXT LINE FROM TIMING CIRCUIT
413
LOAD
415
ADDRESSES TO DRAM
OSD ACK FROM DRAM
401
SYMBOL LINE WIDTH FROM CIM
12
ADD
LINE OFFSET REGISTER
12
423
DATA PATH SELECT FROM INPUT TIMING
DECODE
SYMBOL SIZE FROM CIM
8
12
MPY
ADD
421
MUX
18
18
4
4
OSD DATA FROM DRAM
SYMBOL NUMBER REGISTER
10
417
ADD
18
419
403
ADDRESS SELECT FROM INPUT TIMING CIRCUIT
SYMBOL BASE ADDRESS FROM CIM
18
425
431
ADD
1
18
18
MUX
18
POINTER REGISTER
18
427
LINE START
18
429
LOAD
NEXT LINE FROM TIMING CIRCUIT
VSYNC FROM SYNC CIRCUIT

FIG.19

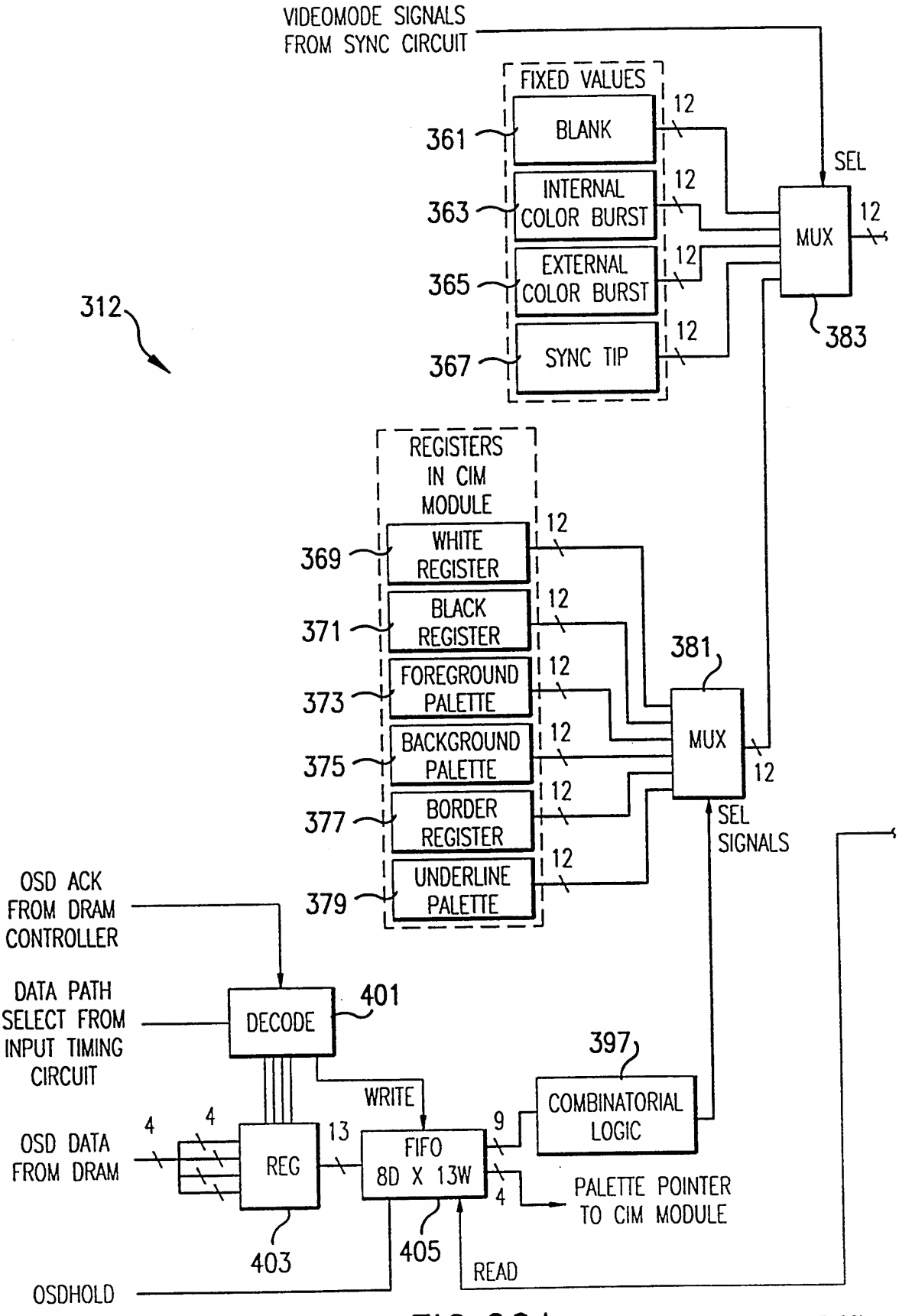
VIDEOMODE SIGNALS FROM SYNC CIRCUIT
FIXED VALUES
BLANK
INTERNAL COLOR BURST
EXTERNAL COLOR BURST
SYNC TIP
361
363
365
367
12
SEL
MUX
383
312
REGISTERS IN CIM MODULE
WHITE REGISTER
BLACK REGISTER
FOREGROUND PALETTE
BACKGROUND PALETTE
BORDER REGISTER
UNDERLINE PALETTE
369
371
373
375
377
379
381
SEL SIGNALS
OSD ACK FROM DRAM CONTROLLER
DATA PATH SELECT FROM INPUT TIMING CIRCUIT
DECODE
401
397
COMBINATORIAL LOGIC
WRITE
OSD DATA FROM DRAM
REG
FIFO 8D X 13W
PALETTE POINTER TO CIM MODULE
403
405
READ
OSDHOLD
4
13
9

FIG.20A

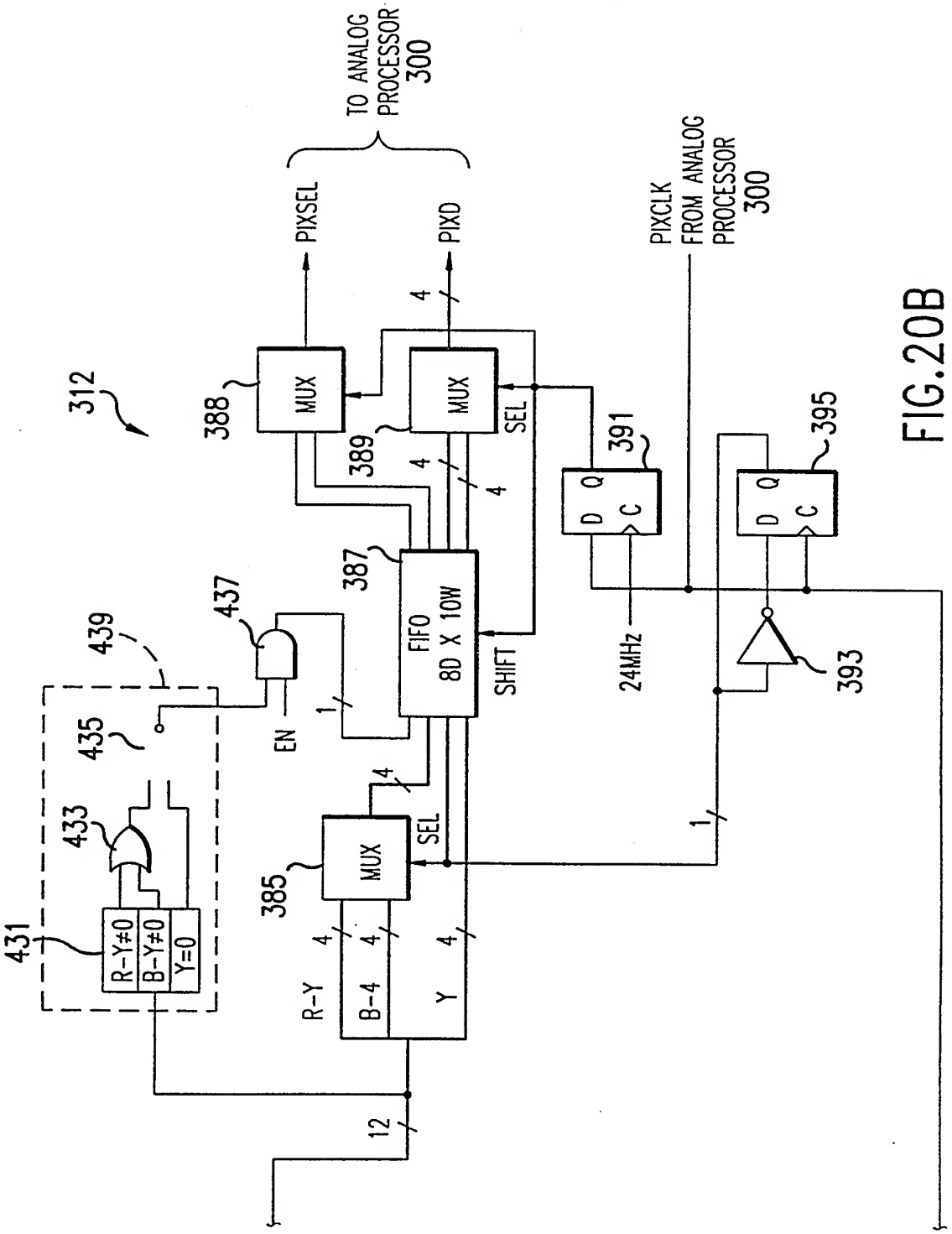
TO ANALOG PROCESSOR 300
PIXSEL
PIXD
PIXCLK FROM ANALOG PROCESSOR 300
312
388
MUX
389
MUX
SEL
391
395
D Q
C
387
FIFO 8D X 10W
SHIFT
437
439
435
EN
24MHz
393
433
385
MUX
SEL
431
R-Y≠0
B-Y≠0
Y=0
R-Y
B-4
Y
4
1
12

FIG.20B

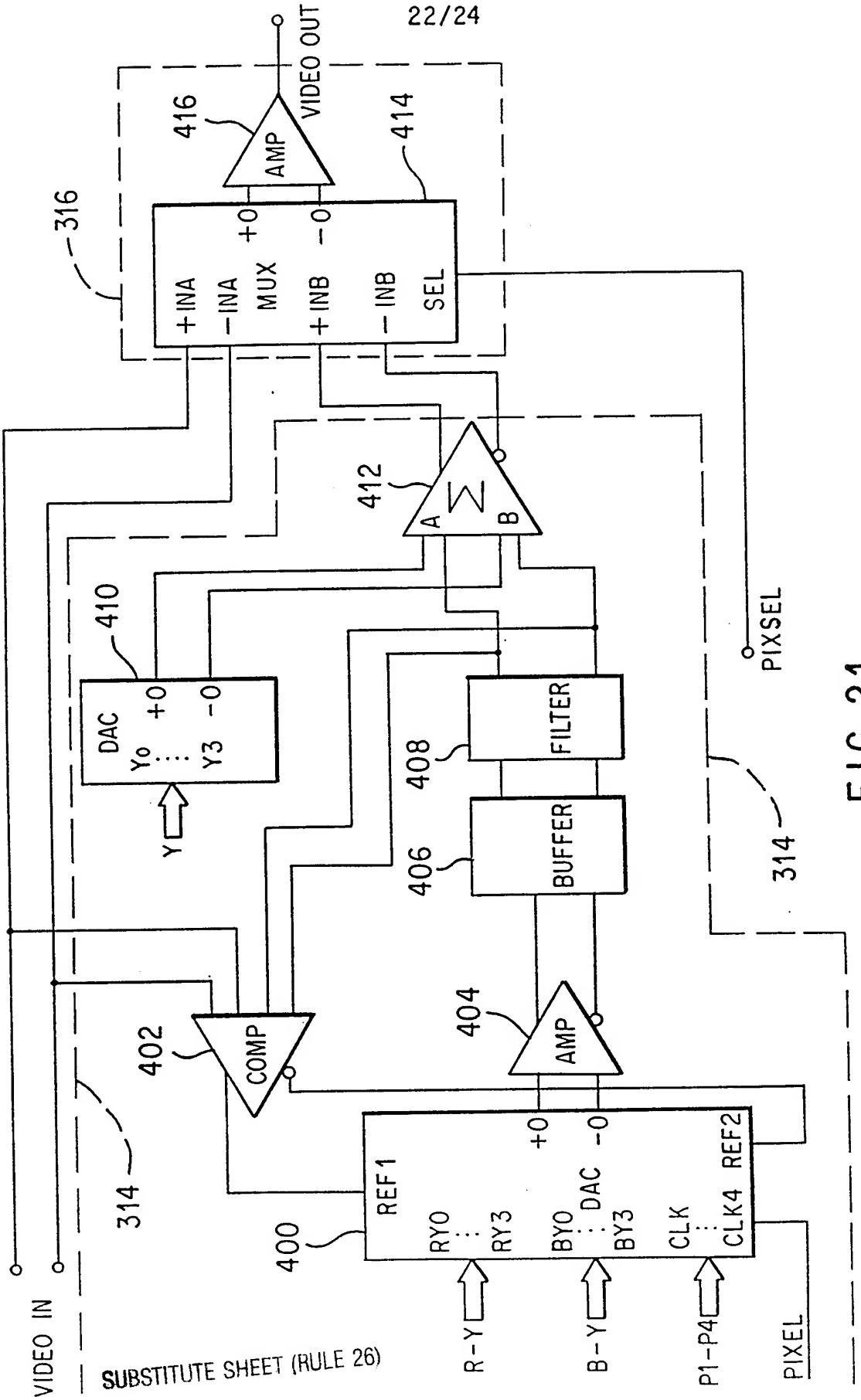
VIDEO OUT
416
AMP
414
316
+INA
-INA
MUX
+INB
-INB
SEL
+0
-0
412
A
B
410
DAC
Y0 : : : Y3
Y
408
FILTER
406
BUFFER
PIXSEL
314
402
COMP
404
AMP
REF1
RY0 : : : RY3
BY0 : : : BY3
DAC
CLK : : : CLK4
REF2
400
VIDEO IN
R-Y
B-Y
P1-P4
PIXEL

FIG. 21

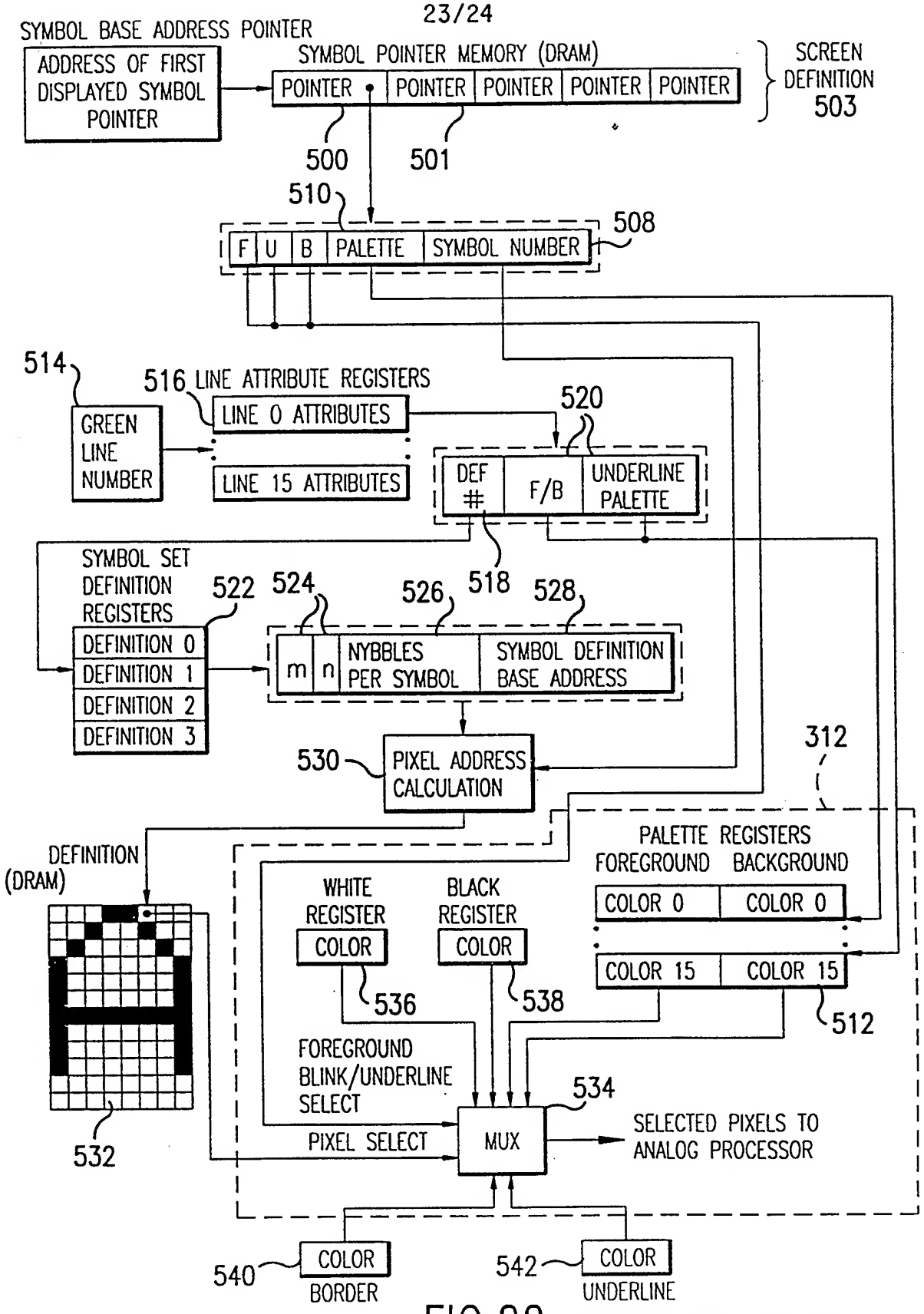
SYMBOL BASE ADDRESS POINTER
ADDRESS OF FIRST DISPLAYED SYMBOL POINTER
SYMBOL POINTER MEMORY (DRAM)
POINTER
POINTER
POINTER
POINTER
POINTER
SCREEN DEFINITION 503
500
501
510
508
F
U
B
PALETTE
SYMBOL NUMBER
514
516 LINE ATTRIBUTE REGISTERS
GREEN LINE NUMBER
LINE 0 ATTRIBUTES
LINE 15 ATTRIBUTES
520
DEF #
F/B
UNDERLINE PALETTE
518
SYMBOL SET DEFINITION REGISTERS
522
524
526
528
DEFINITION 0
DEFINITION 1
DEFINITION 2
DEFINITION 3
m
n
NYBBLES PER SYMBOL
SYMBOL DEFINITION BASE ADDRESS
530
PIXEL ADDRESS CALCULATION
312
DEFINITION (DRAM)
PALETTE REGISTERS
FOREGROUND
BACKGROUND
WHITE REGISTER
COLOR
BLACK REGISTER
COLOR
COLOR 0
COLOR 0
COLOR 15
COLOR 15
512
536
538
FOREGROUND BLINK/UNDERLINE SELECT
534
PIXEL SELECT
MUX
SELECTED PIXELS TO ANALOG PROCESSOR
532
540
COLOR BORDER
542
COLOR UNDERLINE

FIG.22

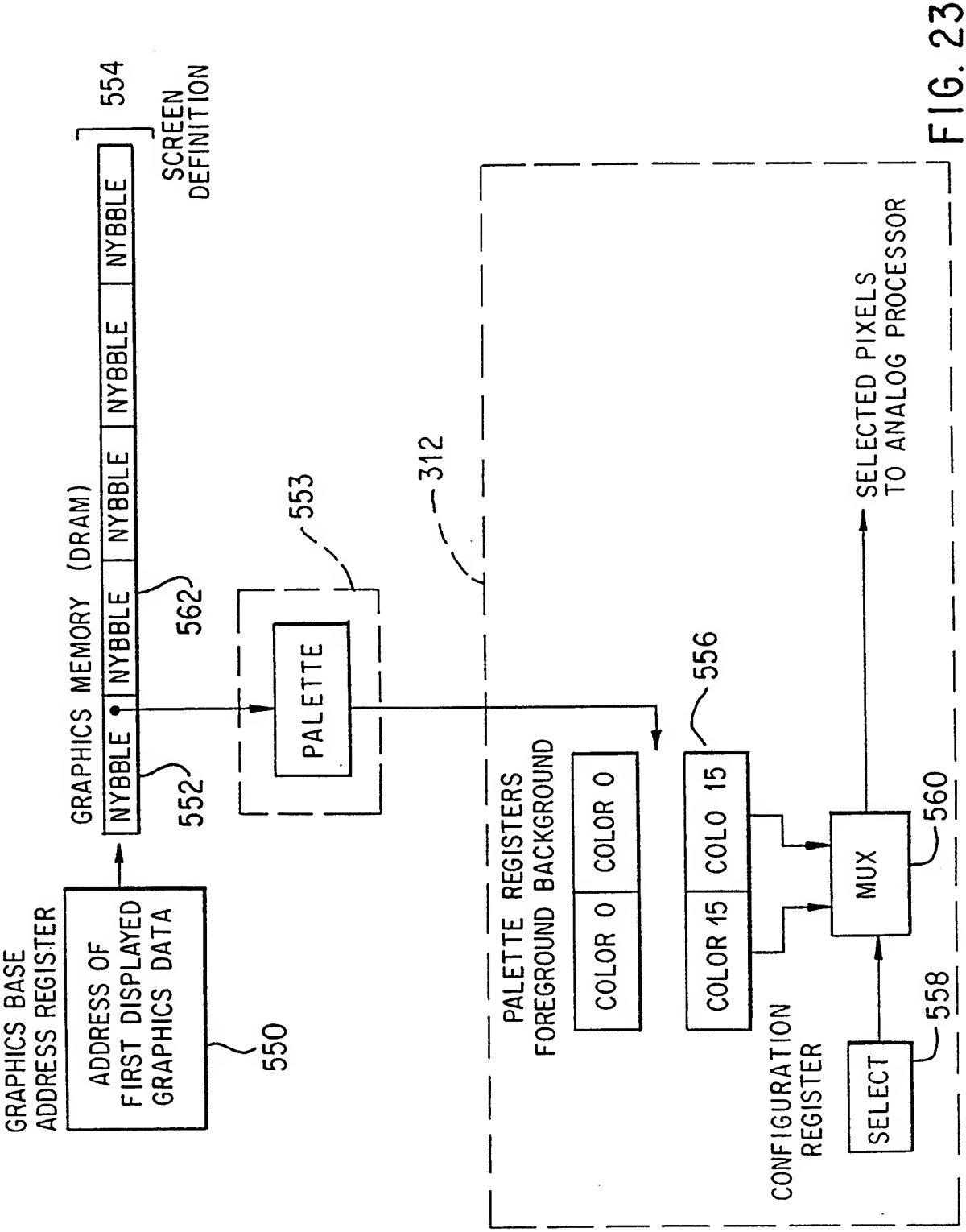
GRAPHICS BASE ADDRESS REGISTER
ADDRESS OF FIRST DISPLAYED GRAPHICS DATA
550
GRAPHICS MEMORY (DRAM)
NYBBLE
NYBBLE
NYBBLE
NYBBLE
NYBBLE
552
562
554
SCREEN DEFINITION
PALETTE
553
312
PALETTE REGISTERS
FOREGROUND BACKGROUND
COLOR 0
COLOR 0
556
COLOR 15
COLO 15
CONFIGURATION REGISTER
SELECT
558
MUX
560
SELECTED PIXELS TO ANALOG PROCESSOR

FIG. 23

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/06340

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H0N 5/262, 5/272, 5/278
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/194, 195, 26, 187, 188, 189, 192, 23; 348/569, 589, 600, 586; 395/147

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,591,845 (KOMATSU ET AL.) 27 MAY 1986, FIGURE 2.	1-40
X	US, A, 4,146,877 (ZIMMER) 27 MARCH 1979, COL. 1, LINES 28-32 AND COL. 3, LINES 39-51.	1-40
X	US, A, 4,489,344 (IKEDA ET AL.) 18 DECEMBER 1984, SEE ABSTRACT.	1-40
X	US, A, 4,951,229 (DINICOLA ET AL.) 21 AUGUST 1990, COL. 2, LINES 29-32.	21, 30, 40

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 22 AUGUST 1994	Date of mailing of the international search report 20 OCT 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer CHERYL COHEN Telephone No. (703) 308-5080

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/06340

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

345/194, 195, 26, 187, 188, 189, 192, 23; 348/569, 589, 600, 586; 395/147

EP0966164A2

Publication Title:

Information transmitting apparatus and method, information receiving apparatus and method, apparatus for providing a computer readable program, and broadcasting system

Abstract:

MPEG video encoders and MPEG audio encoders encode video signals and audio signals, respectively. An SI/EPG data generator generates program information. A transport stream multiplexer multiplexes the program information with video data and audio data. A system controller controls the data output rates of the encoding operations and the multiplexing ratio.

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 966 164 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
22.12.1999 Bulletin 1999/51

(51) Int Cl.[6]: **H04N 7/52**

(21) Application number: **99304701.8**

(22) Date of filing: **16.06.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **18.06.1998 JP 17109698**
18.06.1998 JP 17109798

(71) Applicant: **SONY CORPORATION**
Tokyo 141 (JP)

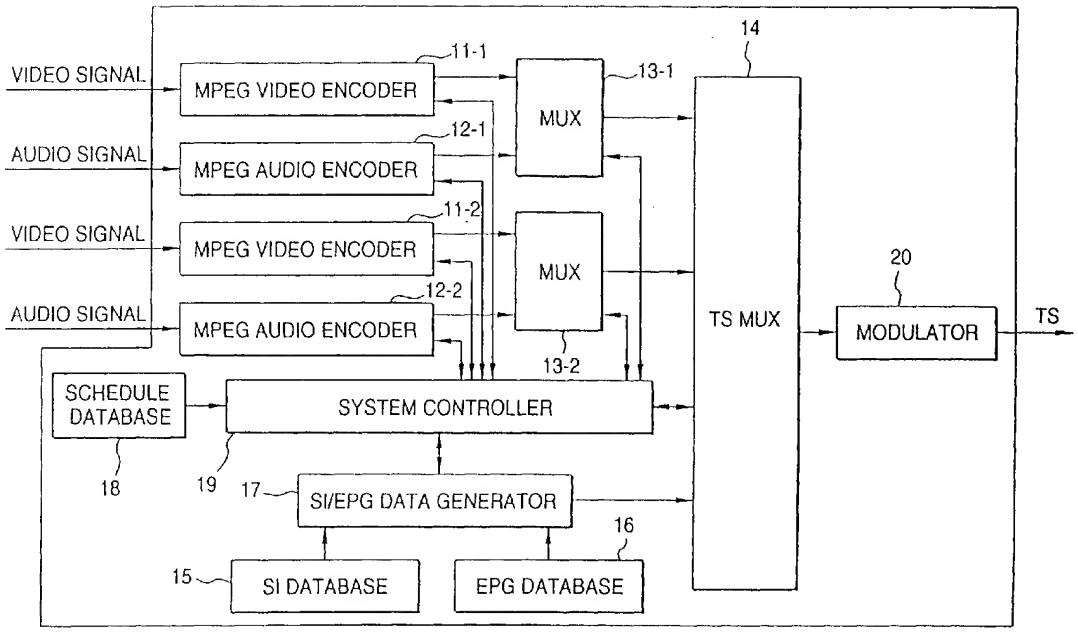
(72) Inventors:
- **Nishina, Yasutomo**
  Shinagawa-ku, Tokyo (JP)
- **Hanai, Tomoyuki**
  Shinagawa-ku, Tokyo (JP)
- **Sato, Masahiko**
  Shinagawa-ku, Tokyo (JP)

(74) Representative: **Turner, James Arthur et al**
D. Young & Co.,
21 New Fetter Lane
London EC4A 1DA (GB)

(54) Information transmitting apparatus and method, information receiving apparatus and method, apparatus for providing a computer readable program, and broadcasting system

(57) MPEG video encoders and MPEG audio encoders encode video signals and audio signals, respectively. An SI/EPG data generator generates program information. A transport stream multiplexer multiplexes the program information with video data and audio data. A system controller controls the data output rates of the encoding operations and the multiplexing ratio.

FIG. 3



EP 0 966 164 A2

Description

[0001] The present invention relates to an information transmitting apparatus and method, an information receiving apparaus and method, a provider, and a broadcasting system.

[0002] In digital broadcasting systems, EPG (electronic program guide) data for providing program information is formed in an EIT (event information table) format according to the rules of DVB/SI (Digital Video Broadcasting/Service Information: EN300468) and multiplexed with other services information (SI) into a transport stream.

[0003] Fig. 1 is a table showing an example of the EIT in which the total transmission rate of EPG information is set at 150 kbps. The EIT consists of a network ID, a TS-ID, a service ID, table IDs, program broadcast hours corresponding to the table IDs, program lengths corresponding to the table IDs, and other data. Further, a program title, genre information, etc. can be described in descriptors together with a broadcast start hour and a program length.

[0004] The EIT generally consists of EPG data of the self station and EPG data of other stations, each of which consists of data of current and next programs, data of programs within 6 hours from the present time, data of programs that are 6-24 hours away, data of programs that are 2-3 days away, and data of programs that are 4-8 days away. The data of programs within 6 hours from the present time, the data of programs that are 6-24 hours away, the data of programs that are 2-3 days away, and the data of programs that are 4-8 days away are generically called schedule EPG data that indicates a program broadcast schedule. Each of those EPG data has its own Table_id (Table_identification code) and a re-transmission cycle. EPG data are transmitted at re-transmission cycles that are set for the respective Table_id data and have respective prescribed transmission rates. The EPG data of current and next programs has a relatively short re-transmission cycle of about several seconds. On the other hand, the schedule EPG data indicating a program broadcast schedule has a re-transmission cycle of about several minutes, which is longer than the re-transmission cycle of the EPG data of current and next programs.

[0005] As shown in Fig. 2, as for the transmission of EPG data, a prescribed EPG data (including prescribed services information) occupation bandwidth is set for the transmission channel bandwidth of a digital broadcasting system. Since priority is given to the transmission of video data and audio data, the EPG data occupation bandwidth does not vary even if a free portion occurs in the occupation bandwidth for the transmission of video data or the occupation bandwidth for the transmission of audio data.

[0006] A viewer takes long time to acquire program information when the data amount of EPG data is large, because EPG data is transmitted to an information receiving apparatus at a constant transmission rate even if a free portion occurs in the occupation bandwidths for the transmission of video data and audio data.

[0007] Further, since schedule EPG data indicating program broadcast schedules has long re-transmission cycles and there is no data indicating their transmission statuses, an information receiving apparatus takes long time to judge the state of the transmission side when the transmission of the schedule EPG data is suspended due to the equipment trouble on the transmission side.

[0008] Various respective aspects and features of the invention are defined in the appended claims.

[0009] Embodiments of the invention can provide an information transmitting apparatus and method, an information receiving apparatus and method, a provider, and a broadcasting system in which the transmission amount of data of program information can be increased when the transmission amounts of video data and audio data can be decreased, and/or an information transmitting apparatus and method, an information receiving apparatus and method, a provider, and a broadcasting system in which the information receiving apparatus can recognize, in a short time, the transmission statuses of schedule EPG data that indicate program broadcast schedules of the transmission side.

[0010] Embodiments of the invention enable acquisition of program information in a short time by increasing the transmission amount of data of program information when the transmission amounts of video data and audio data can be decreased.

[0011] Embodiments of the invention allow an information receiving apparatus to recognize, in a short time, the transmission statuses of schedule EPG data that indicate program broadcast schedules of the transmission side.

[0012] An information transmitting apparatus according to embodiments of the invention comprising multiplexing means for multiplexing a plurality of signals; and control means for controlling a multiplexing ratio among the plurality of signals in the multiplexing means.

[0013] An information transmitting method according to the embodiments of the invention comprises a multiplexing step of multiplexing a plurality of signals; and a control step of controlling a multiplexing ratio among the plurality of signals in the multiplexing step.

[0014] A provider according to embodiments of the invention provides a computer-readable program or medium for causing an information transmitting apparatus to execute a process comprising: a multiplexing step of multiplexing a plurality of signals; and a control step of controlling a multiplexing ratio among the plurality of signals in the multiplexing step.

[0015] An information receiving apparatus according to embodiments of the invention comprises separating means for separating program information that is multiplexed with a video signal and an audio signal; storing means for storing the program information separated by the separating means; and control means for controlling

operations of the separating means and the storing means in accordance with a transmission rate of the program information.

[0016] An information receiving method according to embodiments of the invention comprises a separating step of separating program information that is multiplexed with a video signal and an audio signal; a storing step of storing the program information separated by the separating means; and a control step of controlling operations of the separating step and the storing step in accordance with a transmission rate of the program information.

[0017] A provider according to another embodiment of the invention provides a computer-readable program or medium for causing an information receiving apparatus to execute a process comprising a separating step of separating program information that is multiplexed with a video signal and an audio signal; a storing step of storing the program information separated by the separating means; and a control step of controlling operations of the separating step and the storing step in accordance with a transmission rate of the program information.

[0018] A broadcasting system according to an embodiment of the invention is such that an information transmitting apparatus comprises video encoding means for encoding a video signal; audio encoding means for encoding an audio signal; program information data generating means for generating data of program information; multiplexing means for multiplexing the data of the program information that is output from the program information data generating means with video data that is output from the video encoding means and audio data that is output from the audio encoding means; and control means for controlling a data output rate of the video encoding means, a data output rate of the audio encoding means, a data output rate of the program information data generating means, and a multiplexing ratio among the video data, the audio data, and the data of the program information in the multiplexing means, and that an information receiving apparatus comprises separating means for separating the program information that is multiplexed with the video signal and the audio signal; storing means for storing the program information separated by the separating means; and control means for controlling operations of the separating means and the storing means in accordance with a transmission rate of the program information.

[0019] An information transmitting apparatus according to another embodiment of the invention comprises program information data generating means for generating program information data including information of a transmission status of program information; and multiplexing means for multiplexing the program information data generated by the program information data generating means with an encoded video signal and an encoded audio signal.

[0020] The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

Fig. 1 is a table showing an example of EIT;
Fig. 2 shows how a video data occupation bandwidth, an audio data occupation bandwidth, and an EPG data occupation bandwidth vary with time in relation to a transmission channel bandwidth;
Fig. 3 is a block diagram showing the configuration of an information transmitting apparatus according to an embodiment of the present invention;
Fig. 4 is a table showing an EIT in which the total transmission rate of EPG information is set at 330 kbps;
Fig. 5 shows how a video data occupation bandwidth, an audio data occupation bandwidth, and an EPG data occupation bandwidth vary with time in relation to a transmission channel bandwidth in a case where the transmission rate of EPG data is increased at prescribed time points;
Fig. 6 is a flowchart showing a bandwidth allocation changing process of a system controller;
Fig. 7 is a block diagram showing the configuration of an information receiving apparatus according to an embodiment of the invention;
Fig. 8 is a flowchart showing the operation of an EPG data acquisition process of the information receiving apparatus;
Fig. 9 shows an EIT form that defines a description format of EPG data of current and next programs;
Fig. 10 shows a description of the transmission statuses of schedule EPG data that is made in a descriptor of EPG data of current and next programs and indicates program broadcast schedules;
Fig. 11 is a flowchart showing a process of the information transmitting apparatus for acquiring data of the transmission statuses of schedule EPG data indicating program broadcast schedules; and
Fig. 12 shows a form of a table information table that defines an SI description format.

[0021] Fig. 3 is a block diagram showing the configuration of an information transmitting apparatus according to an embodiment of the invention. The information processing apparatus 1 outputs a transport stream TS based on a plurality of video signals and audio signals that are input externally. An MPEG video encoder 11-1 generates a video elementary stream based on a video signal that is input externally and outputs it to a multiplexer 13-1. An MPEG video encoder 11-2 generates a video elementary stream based on a video signal that is input externally and outputs it to a multiplexer 13-2.

[0022] An MPEG audio encoder 12-1 generates an audio elementary stream based on an audio signal that is input externally and outputs it to the multiplexer 13-1. An MPEG audio encoder 12-2 generates an audio ele-

mentary stream based on an audio signal that is input externally and outputs it to the multiplexer 13-2.

[0023] The multiplexer 13-1 multiplexes a video elementary stream supplied from the MPEG video encoder 11-1 and an audio elementary stream supplied from the MPEG audio encoder 12-1 by incorporating those into packets having a prescribed fixed length, and outputs the packets to a transport stream multiplexer 14. The multiplexer 13-2 multiplexes a video elementary stream supplied from the MPEG video encoder 11-2 and an audio elementary stream supplied from the MPEG audio encoder 12-2 by incorporating those into packets having a prescribed fixed length, and outputs the packets to the transport stream multiplexer 14.

[0024] An SI database 15 supplies system information data stored therein to an SI/EPG data generator 17. An EPG database 16 supplies EPG data stored therein to the SI/EPG data generator 17. The SI/EPG data generator 17 incorporates data that are supplied from the SI database 15 and the EPG database 16 and data indicating the transmission statuses of schedule EPG data that indicate program broadcast schedules into packets of a prescribed fixed length and outputs the packets to the transport stream multiplexer 14.

[0025] A schedule database 18 supplies a system controller 19 with the contents, transmission rates, retransmission cycles, etc. of video data, audio data, and EPG data, respectively, that will be transmitted from the information transmitting apparatus at each time point. Based on the data supplied from the schedule database 18, the system controller 19 manages the states of the MPEG video encoders 11-1 and 11-2 and the MPEG audio encoders 12-1 and 12-2 and controls the bit rates of video elementary streams that are output from the MPEG video encoders 11-1 and 11-2 and audio elementary streams that are output from the MPEG audio encoders 12-1 and 12-2. Further, the system controller 19 controls the amount of packets that are output from the SI/EPG data generator 17. Still further, the system controller 19 controls the multiplexers 13-1 and 13-2 and the transport stream multiplexer 14 to thereby control the video data occupation bandwidth, the audio data occupation bandwidth, and the EPG data occupation bandwidth in relation to the transmission channel bandwidth.

[0026] The transport stream multiplexer 14 multiplexes packets that are supplied from the multiplexers 13-1 and 13-2 and the SI/EPG data generator 17 and outputs a transport stream. A modulator 20 modulates a transport stream that is output from the transport stream multiplexer 14 according to a prescribed modulation scheme and outputs a modulated transport stream TS to, for example, an antenna (not shown) in the case of transmission by radio waves or to a prescribed interface in the case of transmission via a cable.

[0027] Fig. 4 is a table showing an EIT in which the total transmission rate of EPG information is set at 330 kbps. In the EIT shown in Fig. 4, the re-transmission cycle of program information of other stations that are 6-24 hours away is set at 10 seconds that is 1/2 of that of the EIT shown in Fig. 1. The re-transmission cycle of program information of other stations that are 2-3 days away is set at 20 seconds that is 1/3 of that of the EIT shown in Fig. 1. The re-transmission cycle of program information of other stations that are 4-8 days away is set at 30 seconds that is 1/6 of that of the EIT shown in Fig. 1. Therefore, the transmission rate of program information of other stations that are 6-24 hours away in the EIT shown in Fig. 4 is set at 64 kbps, which is two times higher than in the EIT shown in Fig. 1. The transmission rate of program information of other stations that are 2-3 days away in the EIT shown in Fig. 4 is set at 60 kbps, which is three times higher than in the EIT shown in Fig. 1. The transmission rate of program information of other stations that are 4-8 days away in the EIT shown in Fig. 4 is set at 120 kbps, which is six times higher than in the EIT of Fig. 1. A wider transmission channel bandwidth is required to transmit EPG data according to the EIT shown in Fig. 4 than to transmit EPG data according to the EIT shown in Fig. 1.

[0028] Fig. 5 shows how a video data occupation bandwidth, an audio data occupation bandwidth, and EPG data occupation bandwidth vary with time in relation to a transmission channel bandwidth in a case where EPG data is transmitted according to the EIT of Fig. 4 in periods from time 0:00, 2:00, and 4:00 to prescribed time points and according to the EIT of Fig. 1 in the remaining periods. The EPG data occupation bandwidth is wider in the periods from time 0:00, 2:00, and 4:00 to the prescribed time points than in the remaining periods.

[0029] Conversely, the video data occupation bandwidth and the audio data occupation bandwidth are narrower in the periods from time 0:00, 2:00, and 4:00 to the prescribed time points than in the remaining periods. It is necessary to set the video data bit rate and the audio data bit rate lower in the periods from time 0:00, 2:00, and 4:00 to the prescribed time points than in the remaining periods.

[0030] Fig. 6 is a flowchart showing a bandwidth allocation changing process of the system controller 19. At step S11, the system controller 19 reads out, from the schedule database 18, data indicating current allocation of a video data occupation bandwidth, an audio data occupation bandwidth, and an EPG data occupation bandwidth. At step S12, by using the read-out data indicating the bandwidth allocation, the system controller 19 calculates video data transmission rates of the channels corresponding to the MPEG video encoders 11-1 and 11-2, audio data transmission rates of the channels corresponding to the MPEG audio encoders 12-1 and 12-2, and a transmission rate of EPG data.

[0031] At step S13, the system controller 19 sets, in each of the MPEG video encoders 11-1 and 11-2, the MPEG audio encoders 12-1 and 12-2, and the SI/EPG data generator 17, a transmission rate of packets that

are output therefrom. At step S14, the system controller 19 sets operations corresponding to the allocation of a video data occupation bandwidth, an audio data occupation bandwidth, and an EPG data occupation bandwidth in the multiplexers 13-1 and 13-2 and the transport stream multiplexer 14.

[0032] In the above-described manner, the information transmitting apparatus 1 can change the re-transmission cycle of EPG data at prescribed time points based on data that is set in the schedule database 18.

[0033] Fig. 7 is a block diagram showing an information receiving apparatus according to an embodiment of the invention. The information receiving apparatus 2 receives a transport stream that is supplied from a predetermined transmission channel and outputs a prescribed video signal and a prescribed audio signal based on a signal corresponding to a manipulation on a remote controller 3.

[0034] The remote controller 3 transmits a prescribed infrared signal to an infrared rays (Ir) receiver 39 of the information receiving apparatus 2 based on a manipulation such as a channel selection by the user of the information receiving apparatus 2. The Ir receiver 39 outputs, to a system controller 38, prescribed data corresponding to an infrared signal transmitted from the remote controller 3. The system controller 38 supplies a demultiplexer 32 with PID (packet identification data) that is based on a channel selection manipulation by the user, and supplies an EPG controller 35 with data indicating an operation that is based on a display manipulation by the user. The system controller 38 extracts data that is described in the descriptor of EPG data of current and next programs and indicates the transmission statuses of schedule EPG data that indicate program broadcast schedules.

[0035] A demodulator 31 demodulates a transport stream TS that has been modulated according to a prescribed scheme and supplies a demodulated transport stream to the demultiplexer 32. The demultiplexer 32 divides a transport stream, and supplies a video elementary stream obtained from packets having prescribed PID to a video encoder 33, an audio elementary stream obtained from packets having prescribed PID to an audio decoder 34, EPG data to the EPG controller 35, and SI data to the system controller 38.

[0036] The video decoder 33 decodes a received video elementary stream and outputs a video signal according to a prescribed scheme to a display controller 37. The audio decoder 34 decodes a received audio elementary stream and outputs an audio signal to the outside.

[0037] The EPG controller 35 stores EPG data that is supplied from the demultiplexer 32 in an EPG memory 36. The EPG controller 35 reads out data stored in the EPG memory 36 under the control of the system controller 38 and outputs the read-out data to the display controller 37 according to a prescribed scheme. The display controller 37 outputs a prescribed video signal to the outside based on signals supplied from the video decoder 33 and the EPG controller 35.

[0038] Fig. 8 is a flowchart showing the operation of an EPG data acquisition process of the information receiving apparatus 2. At step S21, the system controller 38 judges whether there has occurred an EPG data acquisition request. If there has occurred an EPG data acquisition request, the process goes to step S22, where it is judged whether the setting of the system controller 38 by the user's manipulating the remote controller 3 is such that EPG data should be acquired only at the time of rate increase (the total transfer rate of EPG information is increased). If it is judged at step S22 that EPG data should be acquired only at the time of rate increase, the process goes to step S23, where the system controller 38 judges whether it has set data of a rate increase period in the EPG controller 35.

[0039] If it is judged at step S23 that no data of a rate increase period has been set in the EPG controller 35, the process goes to step S24, where the system controller 38 searches for data of an EPG data rate increase period that is included in SI data supplied from the demultiplexer 32. At step S25, the system controller 38 judges whether data of a rate increase period could be retrieved. If it is judged that data of a rate increase period could be retrieved, the process goes to step S27, where the system controller 38 sets the data of a rate increase period in the EPG controller 35 as data acquisition time. Then, the process goes to step S28.

[0040] If it is judged at step S25 that no data of a rate increase period could be retrieved, the system controller 38 sets default data acquisition time in the EPG controller 35. Then, the process goes to step S28.

[0041] At step S28, the EPG controller 35 judges whether the present time is the thus-set data acquisition time. If it is judged that the present time is the thus-set data acquisition time, the process goes to step S29, where EPG data is acquired and stored in the EPG memory 36.

[0042] If it is judged at step S28 that the present time is not the thus-set data acquisition time, the process is finished.

[0043] If it is judged at step S23 that data for a rate increase period has been set in the EPG controller 35, the process goes to step S28.

[0044] If it is judged at step S22 that EPG data should be acquired also at time other than the time of rate increase, the process goes to step S29, where EPG data is acquired and stored in the EPG memory 36.

[0045] If it is judged at step S21 that there has occurred no EPG data acquisition request, the process is finished.

[0046] As described above, the information receiving apparatus 2 can acquire EPG data only in rate increase periods. Periods when the total transmission rate of EPG information should be increased may be determined by management and the information receiving apparatus 2 may be caused to operate in accordance

with the management.

[0047] Fig. 9 shows an EIT form that defines a description format of EPG data of current and next programs. A table ID (table_id) on the second line of the EIT to a last table ID (last_table_id) on the 16th line are a header portion to be used for identification of this EIT. An event ID (event_id) on the 18th line and the following items are for description of transmission information relating to the current and next programs, and has a loop structure to allow repetitive description of transmission information relating to a plurality of programs. The transmission information relating to the current and next programs consists of program start hours, program lengths, and other information. Information relating to a program such as a program title or a genre of the program can be described in a descriptor on the 25th line.

[0048] Fig. 10 shows a description of the transmission statuses of schedule EPG data that are described in the descriptor of EPG data of current and next programs and indicate program broadcast schedules. To describe the statuses of a plurality of schedule EPG data indicating program broadcast schedules, the second to sixth lines have a loop structure. A table ID (table_id) on the third line indicates an ID corresponding to schedule EPG data indicating a program broadcast schedule. A status flag (status_flag) on the fourth line indicates that the information transmitting apparatus 1 is transmitting schedule EPG data indicating the corresponding program broadcast schedule if it has a value "1," and indicates that the information transmitting apparatus 1 is not doing so if it has a value "0." A version number (version_number) on the fifth line indicates a value that allows the information receiving apparatus 2 to recognize whether the content is the same as in an already acquired descriptor.

[0049] As described above, by reading out the contents of the descriptor of EPG data of current and next programs, the information receiving apparatus 2 can recognize, at the re-transmission cycle of the EPG data of current and next programs, the transmission statuses of schedule EPG data indicating program broadcast schedules.

[0050] Fig. 11 is a flowchart showing a process of the information receiving apparatus 2 for acquiring data of the transmission statuses of schedule EPG data indicating program broadcast schedules. At step S11, the system controller 38 reads out the descriptor of EPG data of current and next programs. At step S12, the system controller 38 judges whether the descriptor of the EPG data of current and next programs includes data that indicates the transmission status of schedule EPG data indicating a program broadcast schedule. If it is judged that the descriptor of the EPG data of current and next programs includes data that indicates the transmission status of schedule EPG data indicating a program broadcast schedule, the process goes to step S13, where a table ID and a version number is read out.

[0051] At step S14, the system controller 38 judges whether there exists already acquired data relating to the transmission status of schedule EPG data indicating a program broadcast schedule corresponding to the table ID that was read out at step S13. If it is judged that there exists already acquired data relating to the transmission status of schedule EPG data indicating a program broadcast schedule, the process goes to step S15. At step S15, the system controller 38 judges whether the version number has been updated by comparing the version number that is included in the already acquired data relating to the transmission status of schedule EPG data indicating a program broadcast schedule with the version number read out at step S13. If it is judged that the version number has been updated, the process goes to step S16, where the system controller 38 reads out the data of the transmission status of schedule EPG data indicating a program broadcast schedule and stores it in a prescribed register inside the system controller 38.

[0052] If it is judged at step S14 that there is no already acquired data relating to the transmission status of schedule EPG data indicating a program broadcast schedule, the process goes to step S16, where the system controller 38 reads out the data of the transmission status of schedule EPG data indicating a program broadcast schedule and stores it in a prescribed register inside the system controller 38.

[0053] If it is judged at step S15 that the version number has not been updated yet, the process goes to step S17.

[0054] At step S17, the system controller 38 judges whether there exists next data that indicates the transmission status of schedule EPG data indicating a program broadcast schedule. If it is judged that there exists next data that indicates a transmission status of schedule EPG data indicating a program broadcast schedule, the process returns to step S13 to repeat execution of step S13 and the following steps.

[0055] If it is judged at step S12 that the descriptor of the EPG data of current and next programs includes no data that indicates a transmission state of schedule EPG data indicating a program broadcast schedule, the process is finished. If it is judged at step S17 that there exists no next data that indicates a transmission state of schedule EPG data indicating a program broadcast schedule, the process is finished.

[0056] As described above, the information receiving apparatus 2 can recognize, at the re-transmission cycle of EPG data of current and next programs, the transmission statuses of schedule EPG data indicating latest program broadcast schedules by reading out the contents of the descriptor of the EPG data of current and next programs.

[0057] Fig. 12 shows a form of a table information table (TIT) that defines a description format of SI that indicates presence/absence of each piece of table information of an EIT or the like, a transmission cycle of EPG data, an updating date and time of EPG data, etc. The descriptions from a table ID (table_id) on the second line

of the TIT to a last table ID (last_table_id) on the 16th line represent a header portion to be used for identification of this TIT. A table ID (table_id) on the 18th line and the following items describe transmission information relating to an EIT and has a loop structure to enable repetitive description of transmission information relating to a plurality of EITs. The transmission information relating to an EIT consists of a re-transmission cycle of the EIT, last updating time, a transmission status of the EIT, etc.

[0058] By utilizing transmission information relating to EITs that is described in SI according to the above TIT description format, the information receiving apparatus 2 can recognize the transmission statuses of schedule EPG data indicating program broadcast schedules by executing a process equivalent to the one shown in Fig. 11.

[0059] As described above, the information receiving apparatus 2 can recognize, in a short time, the transmission statuses of schedule EPG data indicating transmission-side program broadcast schedules.

[0060] In this specification, the term "system" means the entire apparatus that consists of a plurality of apparatuses.

[0061] Not only recording media such as a magnetic disk, a CD-ROM, a solid-state memory but also communication media such as a network and a satellite can be used as a provider for providing a user with a computer program for execution of the above-described process.

Claims

1. An information transmitting apparatus which transmits a plurality of signals after multiplexing those, comprising:

   multiplexing means for multiplexing the plurality of signals; and
   control means for controlling a multiplexing ratio among the plurality of signals in the multiplexing means.

2. The information transmitting apparatus according to claim 1, wherein the transmitting apparatus transmits the plurality of signals as a single transport stream.

3. The information transmitting apparatus according to claim 1, further comprising database means for providing data that relates to transmission rates of the plurality of signals at each time point, wherein the control means controls the multiplexing ratio while referring to the database means.

4. The information transmitting apparatus according to claim 1, further comprising encoding means for one of the plurality of signals, wherein the control means controls an output rate of the encoding means.

5. The information transmitting apparatus according to claim 1, wherein the plurality of signals are program information, a video signal, and an audio signal.

6. An information transmitting apparatus which transmits program information after multiplexing it with a video signal and an audio signal, comprising:

   video encoding means for encoding the video signal;
   audio encoding means for encoding the audio signal;
   program information data generating means for generating data of the program information;
   multiplexing means for multiplexing the data of the program information that is output from the program information data generating means with video data that is output from the video encoding means and audio data that is output from the audio encoding means; and
   control means for controlling a data output rate of the video encoding means, a data output rate of the audio encoding means, a data output rate of the program information data generating means, and a multiplexing ratio among the video data, the audio data, and the data of the program information in the multiplexing means.

7. An information transmitting method for transmitting a plurality of signals after multiplexing those, comprising:

   a multiplexing step of multiplexing the plurality of signals; and
   a control step of controlling a multiplexing ratio among the plurality of signals in the multiplexing step.

8. The information transmitting method according to claim 7, wherein the control step controls the multiplexing ratio while referring to data that relates to transmission rates of the plurality of signals at each time point.

9. The information transmitting method according to claim 7, wherein the plurality of signals are program information, a video signal, and an audio signal.

10. An information transmitting method for transmitting program information after multiplexing it with a video signal and an audio signal, characterized by comprising:

    a video encoding step of encoding the video

signal;
an audio encoding step of encoding the audio signal;
a program information data generating step of generating data of the program information;
a multiplexing step of multiplexing the data of the program information that is output by the program information data generating step with video data that is output by the video encoding step and audio data that is output by the audio encoding step; and
a control step of controlling a data output rate of the video encoding step, a data output rate of the audio encoding step, a data output rate of the program information data generating step, and a multiplexing ratio among the video data, the audio data, and the data of the program information in the multiplexing step.

11. A provider for providing a computer-readable program for causing an information transmitting apparatus which transmits a plurality of signals after multiplexing those to execute a process comprising:

a multiplexing step of multiplexing the plurality of signals; and
a control step of controlling a multiplexing ratio among the plurality of signals in the multiplexing step.

12. The provider according to claim 11, wherein the control step controls the multiplexing ratio while referring to data that relates to transmission rates of the plurality of signals at each time point.

13. The provider according to claim 11, wherein the plurality of signals are program information, a video signal, and an audio signal.

14. A provider for providing a computer-readable program for causing an information transmitting apparatus which transmits program information after multiplexing it with a video signal and an audio signal to execute a process comprising:

a video encoding step of encoding the video signal;
an audio encoding step of encoding the audio signal;
a program information data generating step of generating data of the program information;
a multiplexing step of multiplexing the data of the program information that is output by the program information data generating step with video data that is output by the video encoding step and audio data that is output by the audio encoding step; and
a control step of controlling a data output rate of the video encoding step, a data output rate of the audio encoding step, a data output rate of the program information data generating step, and a multiplexing ratio among the video data, the audio data, and the data of the program information in the multiplexing step.

15. An information receiving apparatus which receives program information that is multiplexed with a video signal and an audio signal and displays the program information together with the video signal, comprising:

separating means for separating the program information that is multiplexed with the video signal and the audio signal;
storing means for storing the program information separated by the separating means; and
control means for controlling operations of the separating means and the storing means in accordance with a transmission rate of the program information.

16. The information receiving apparatus according to claim 15, wherein the control means controls the operations of the separating means and the storing means so that the program information is acquired only in a prescribed period when the transmission rate of the program information is high.

17. An information receiving method for receiving program information that is multiplexed with a video signal and an audio signal and displaying the program information together with the video signal, comprising:

a separating step of separating the program information that is multiplexed with the video signal and the audio signal;
a storing step of storing the program information separated by the separating means; and
a control step of controlling operations of the separating step and the storing step in accordance with a transmission rate of the program information.

18. The information receiving method according to claim 17, wherein the control step controls the operations of the separating means and the storing means so that the program information is acquired only in a prescribed period when the transmission rate of the program information is high.

19. A provider for providing a computer-readable program for causing an information receiving apparatus which receives program information that is multiplexed with a video signal and an audio signal and displays the program information together with the

video signal to execute a process comprising:

a separating step of separating the program information that is multiplexed with the video signal and the audio signal;
a storing step of storing the program information separated by the separating means; and
a control step of controlling operations of the separating step and the storing step in accordance with a transmission rate of the program information.

20. The provider according to claim 19, wherein the control step controls the operations of the separating means and the storing means so that the program information is acquired only in a prescribed period when the transmission rate of the program information is high.

21. A broadcasting system having an information transmitting apparatus which transmits program information after multiplexing it with a video signal and an audio signal and an information receiving apparatus which receives the program information that is multiplexed with the video signal and the audio signal and displays the program information together with the video signal, the information transmitting apparatus comprising:

video encoding means for encoding the video signal;
audio encoding means for encoding the audio signal;
program information data generating means for generating data of the program information;
multiplexing means for multiplexing the data of the program information that is output from the program information data generating means with video data that is output from the video encoding means and audio data that is output from the audio encoding means; and
control means for controlling a data output rate of the video encoding means, a data output rate of the audio encoding means, a data output rate of the program information data generating means, and a multiplexing ratio among the video data, the audio data, and the data of the program information in the multiplexing means, and the information receiving apparatus comprising:
separating means for separating the program information that is multiplexed with the video signal and the audio signal;
storing means for storing the program information separated by the separating means; and
control means for controlling operations of the separating means and the storing means in accordance with a transmission rate of the program information.

22. An information transmitting apparatus which transmits program information after multiplexing it with a video signal and an audio signal, comprising:

program information data generating means for generating program information data including information of a transmission status of the program information; and
multiplexing means for multiplexing the program information data generated by the program information data generating means with an encoded version of the video signal and an encoded version of the audio signal.

23. An information transmitting method for transmitting program information after multiplexing it with a video signal and an audio signal, comprising:

a program information data generating step of generating program information data including information of a transmission status of the program information; and
a multiplexing step of multiplexing the program information data generated by the program information data generating means with an encoded version of the video signal and an encoded version of the audio signal.

24. A provider for providing a computer-readable program for causing an information transmitting apparatus which transmits program information after multiplexing it with a video signal and an audio signal to execute a process comprising:

a program information data generating step of generating program information data including information of a transmission status of the program information; and
a multiplexing step of multiplexing the program information data generated in the program information data generating means with an encoded version of the video signal and an encoded version of the audio signal.

25. An information receiving apparatus which receives program information that is multiplexed with a video signal and an audio signal and displays the program information together with the video signal, comprising:

separating means for separating program information data that is multiplexed with the video signal and the audio signal; and
extracting means for extracting information of a transmission status of the program information that is included in the program information

data separated by the separating means.

26. An information receiving method for receiving program information that is multiplexed with a video signal and an audio signal and displaying the program information together with the video signal, comprising:

a separating step of separating program information data that is multiplexed with the video signal and the audio signal; and
an extracting step of extracting information of a transmission status of the program information that is included in the program information data separated by the separating means.

27. A provider for providing a computer-readable program for causing an information receiving apparatus which receives program information that is multiplexed with a video signal and an audio signal and displays the program information together with the video signal to execute a process comprising:

a separating step of separating program information data that is multiplexed with the video signal and the audio signal; and
an extracting step of extracting information of a transmission status of the program information that is included in the program information data separated by the separating means.

28. A broadcasting system having an information transmitting apparatus which transmits program information after multiplexing it with a video signal and an audio signal and an information receiving apparatus which receives the program information that is multiplexed with the video signal and the audio signal and displays the program information together with the video signal, the information transmitting apparatus comprising:

program information data generating means for generating program information data including information of a transmission status of the program information; and
multiplexing means for multiplexing the program information data generated by the program information data generating means with an encoded version of the video signal and an encoded version of the audio signal, and the information receiving apparatus comprising:
separating means for separating the program information data that is multiplexed with the video signal and the audio signal; and
extracting means for extracting information of a transmission status of the program information that is included in the program information data separated by the separating means.

FIG. 1

KIND OF PROGRAM INFORMATION (EIT)		Table_id	RE-TRANSMISSION CYCLE (sec)	TRANSMISSION RATE (kbps)
PROGRAM INFORMATION OF SELF STATION	CURRENT, NEXT	0x4E	3	1
	WITHIN 6 HOURS FROM PRESENT TIME	0x50	5	5
	6-24 HOURS AWAY	0x51	10	10
	2-3 DAYS AWAY	0x52	20	10
	4-8 DAYS AWAY	0x53	60	10
PROGRAM INFORMATION OF ANOTHER STATION	CURRENT, NEXT	0x4F	3	10
	WITHIN 6 HOURS FROM PRESENT TIME	0x60	5	32
	6-24 HOURS AWAY	0x61	20	32
	2-3 DAYS AWAY	0x62	60	20
	4-8 DAYS AWAY	0x63	180	20
TOTAL				150

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FIG. 2

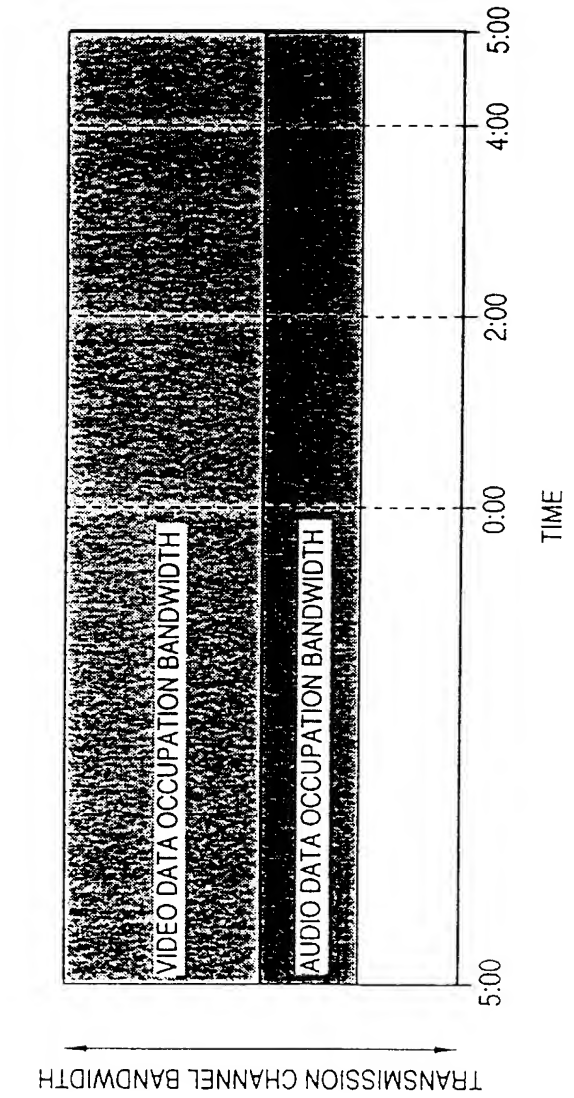
VIDEO DATA OCCUPATION BANDWIDTH
AUDIO DATA OCCUPATION BANDWIDTH
0:00
2:00
4:00
5:00
5:00
TIME
TRANSMISSION CHANNEL BANDWIDTH

FIG. 3

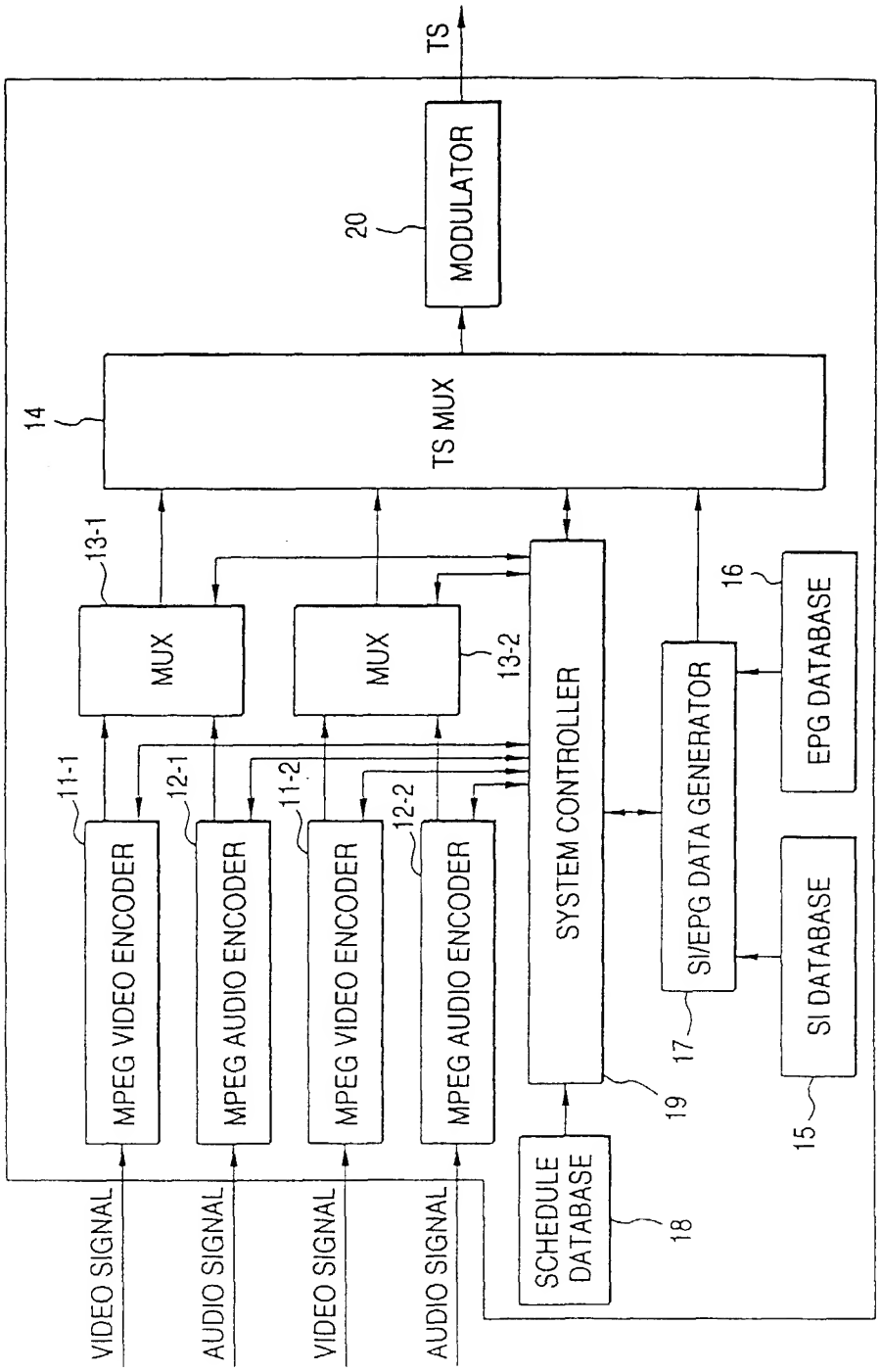
TS
20
MODULATOR
14
TS MUX
13-1
MUX
13-2
MUX
11-1
12-1
11-2
12-2
MPEG VIDEO ENCODER
MPEG AUDIO ENCODER
MPEG VIDEO ENCODER
MPEG AUDIO ENCODER
SYSTEM CONTROLLER
SI/EPG DATA GENERATOR
16
EPG DATABASE
SI DATABASE
15
17
19
SCHEDULE DATABASE
18
VIDEO SIGNAL
AUDIO SIGNAL
VIDEO SIGNAL
AUDIO SIGNAL

FIG. 4

KIND OF PROGRAM INFORMATION		TABLE_ ID	RE-TRANSMISSION CYCLE (Sec)	TRANSMISSION RATE (kbps)
PROGRAM INFORMATION OF SELF STATION	CURRENT, NEXT	0×4E	3	1
	WITHIN 6 HOURS FROM PRESENT TIME	0×50	5	5
	6-24 HOURS AWAY	0×51	10	10
	2-3 DAYS AWAY	0×52	20	10
	4-8 DAYS AWAY	0×53	30	30
PROGRAM INFORMATION OF ANOTHER STATION	CURRENT, NEXT	0×4F	3	10
	WITHIN 6 HOURS FROM PRESENT TIME	0×60	5	30
	6-24 HOURS AWAY	0×61	10	64
	2-3 DAYS AWAY	0×62	20	60
	4-8 DAYS AWAY	0×63	30	120
TOTAL				330

FIG. 5

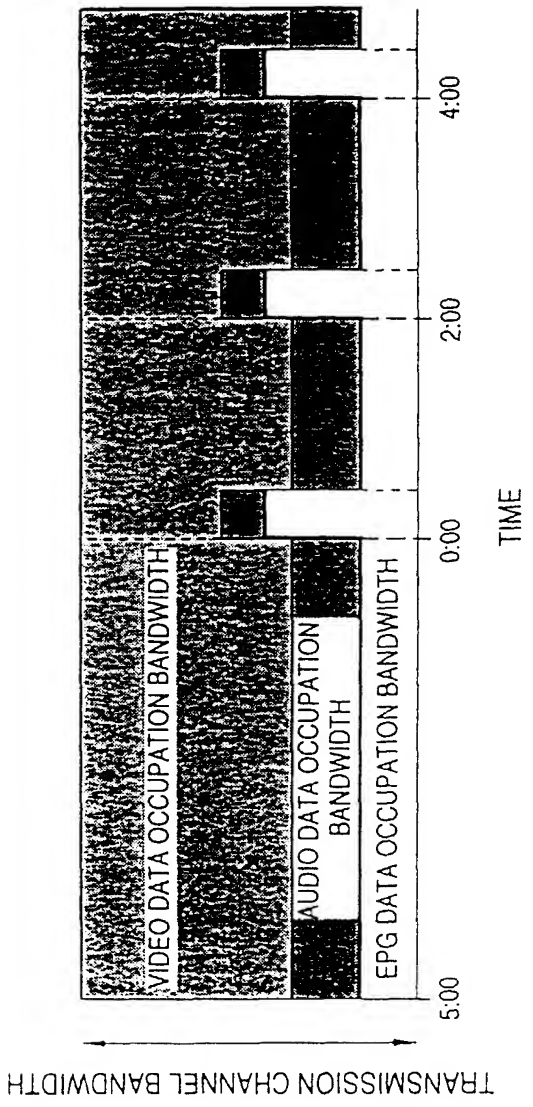
VIDEO DATA OCCUPATION BANDWIDTH
AUDIO DATA OCCUPATION BANDWIDTH
EPG DATA OCCUPATION BANDWIDTH
5:00
0:00
2:00
4:00
TIME
TRANSMISSION CHANNEL BANDWIDTH

FIG. 6

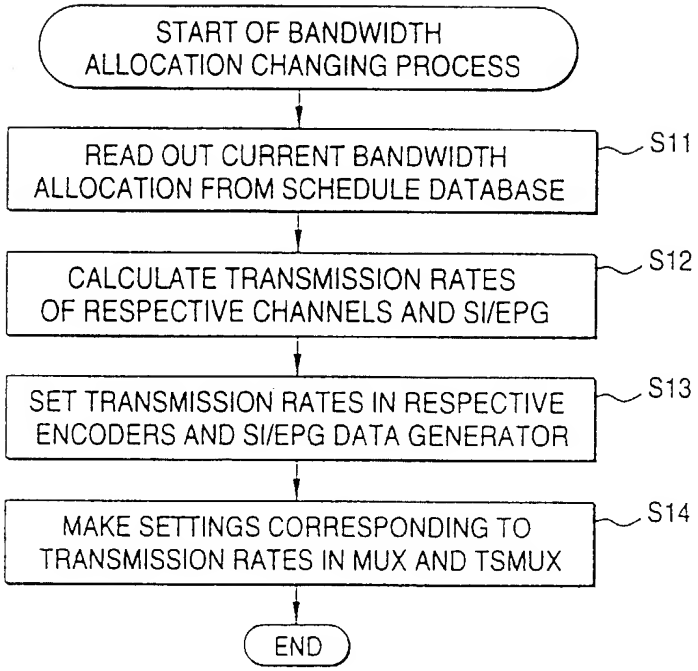
START OF BANDWIDTH ALLOCATION CHANGING PROCESS
READ OUT CURRENT BANDWIDTH ALLOCATION FROM SCHEDULE DATABASE
S11
CALCULATE TRANSMISSION RATES OF RESPECTIVE CHANNELS AND SI/EPG
S12
SET TRANSMISSION RATES IN RESPECTIVE ENCODERS AND SI/EPG DATA GENERATOR
S13
MAKE SETTINGS CORRESPONDING TO TRANSMISSION RATES IN MUX AND TSMUX
S14
END

FIG. 7

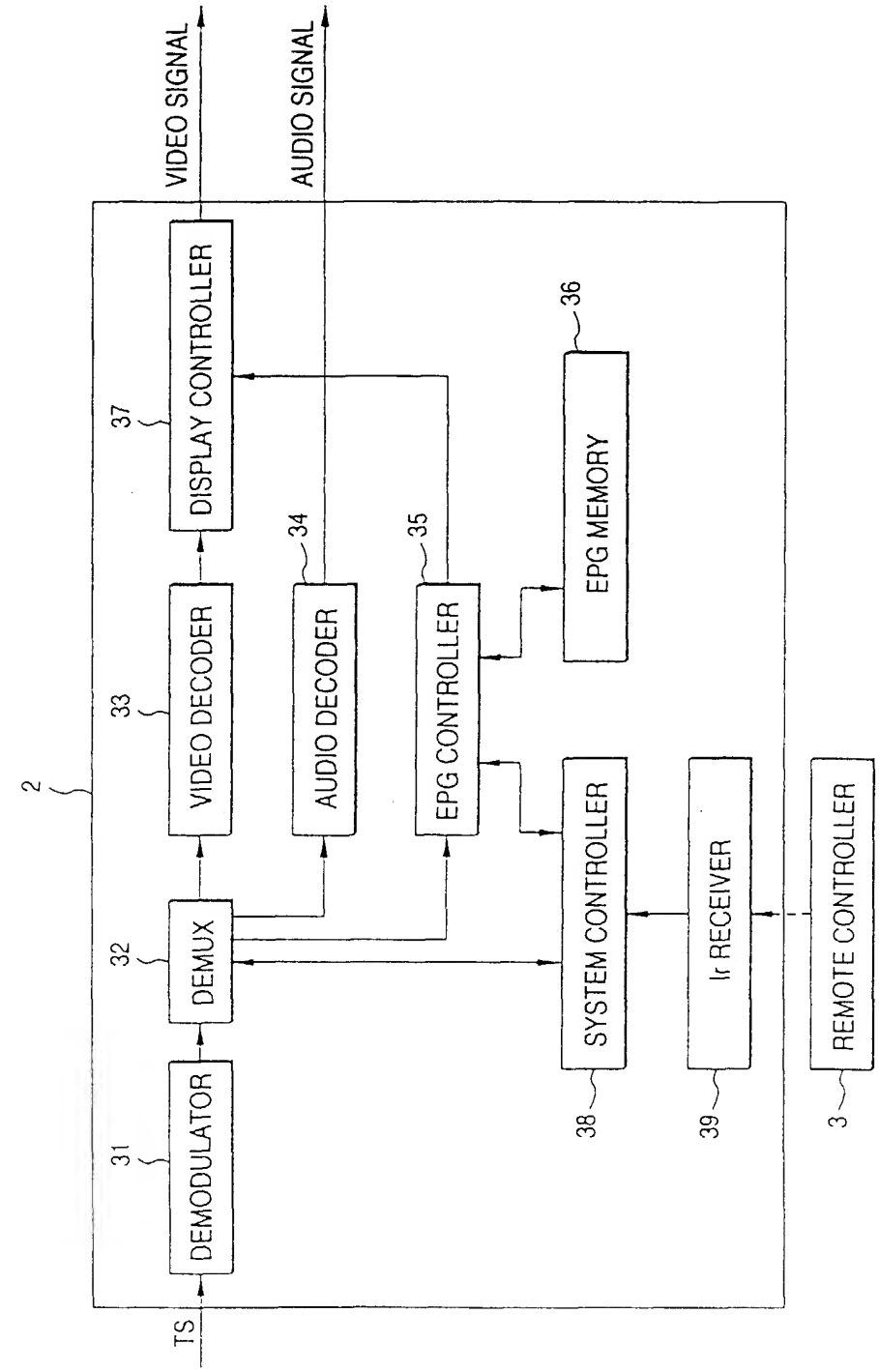
TS
2
DEMODULATOR
31
DEMUX
32
VIDEO DECODER
33
AUDIO DECODER
34
EPG CONTROLLER
35
DISPLAY CONTROLLER
37
EPG MEMORY
36
SYSTEM CONTROLLER
38
Ir RECEIVER
39
REMOTE CONTROLLER
3
VIDEO SIGNAL
AUDIO SIGNAL

FIG. 8

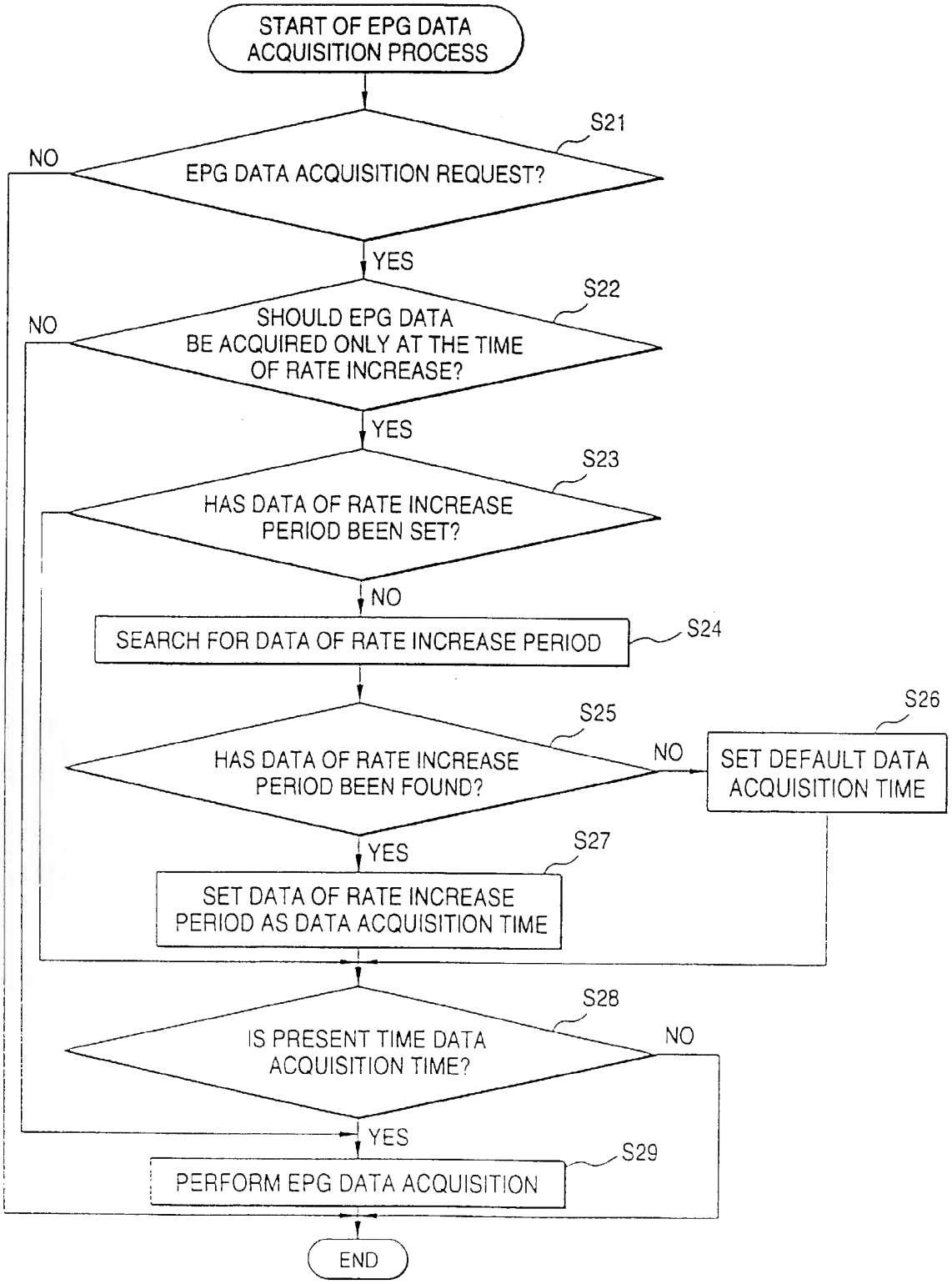
START OF EPG DATA ACQUISITION PROCESS
S21
EPG DATA ACQUISITION REQUEST?
NO
YES
S22
SHOULD EPG DATA BE ACQUIRED ONLY AT THE TIME OF RATE INCREASE?
NO
YES
S23
HAS DATA OF RATE INCREASE PERIOD BEEN SET?
NO
SEARCH FOR DATA OF RATE INCREASE PERIOD
S24
S25
HAS DATA OF RATE INCREASE PERIOD BEEN FOUND?
NO
S26
SET DEFAULT DATA ACQUISITION TIME
YES
S27
SET DATA OF RATE INCREASE PERIOD AS DATA ACQUISITION TIME
S28
IS PRESENT TIME DATA ACQUISITION TIME?
NO
YES
S29
PERFORM EPG DATA ACQUISITION
END

FIG. 9

SYNTAX	NUMBER OF BITS	MNEMONIC
event_information () {		
table_id	8	uimsbf
section_syntax_indicator	1	bslbf
reserved_future_use	1	bslbf
reserved	2	bslbf
section_length	12	uimsbf
service_id	16	uimsbf
reserved	2	bslbf
version_number	5	uimsbf
current_next_indicator	1	bslbf
section_number	8	uimsbf
last_section_number	8	uimsbf
transport_stream_id	16	uimsbf
original_network_id	16	uimsbf
segment_last_section_number	8	uimsbf
last_table_id	8	uimsbf
for (i=0; i<N; i++) {		
event_id	16	uimsbf
start_time	40	bslbf
duration	24	uimsbf
running_status	3	uimsbf
free_CA_mode	1	bslbf
descriptors_loop_length	12	uimsbf
for (i=0; i<N; i++) {		
}		
}		
CRC_32	32	rpchof
}		

FIG. 10

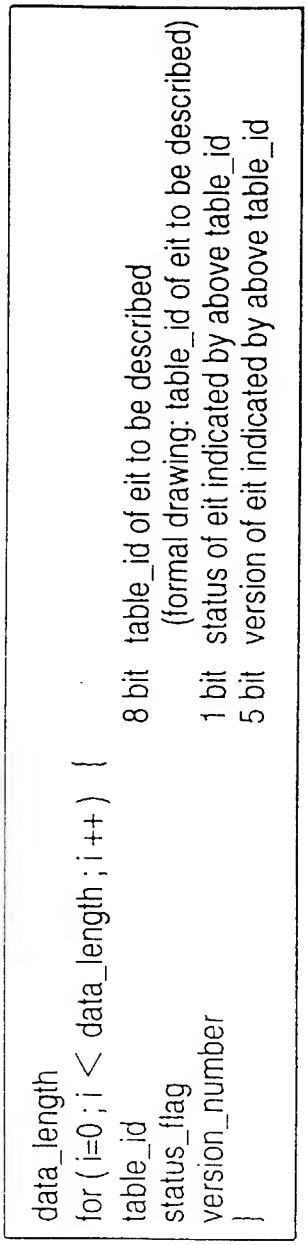
data_length
for (i=0 ; i < data_length ; i ++) {
table_id
8 bit table_id of eit to be described
(formal drawing: table_id of eit to be described)
status_flag
1 bit status of eit indicated by above table_id
version_number
5 bit version of eit indicated by above table_id
}

FIG. 11

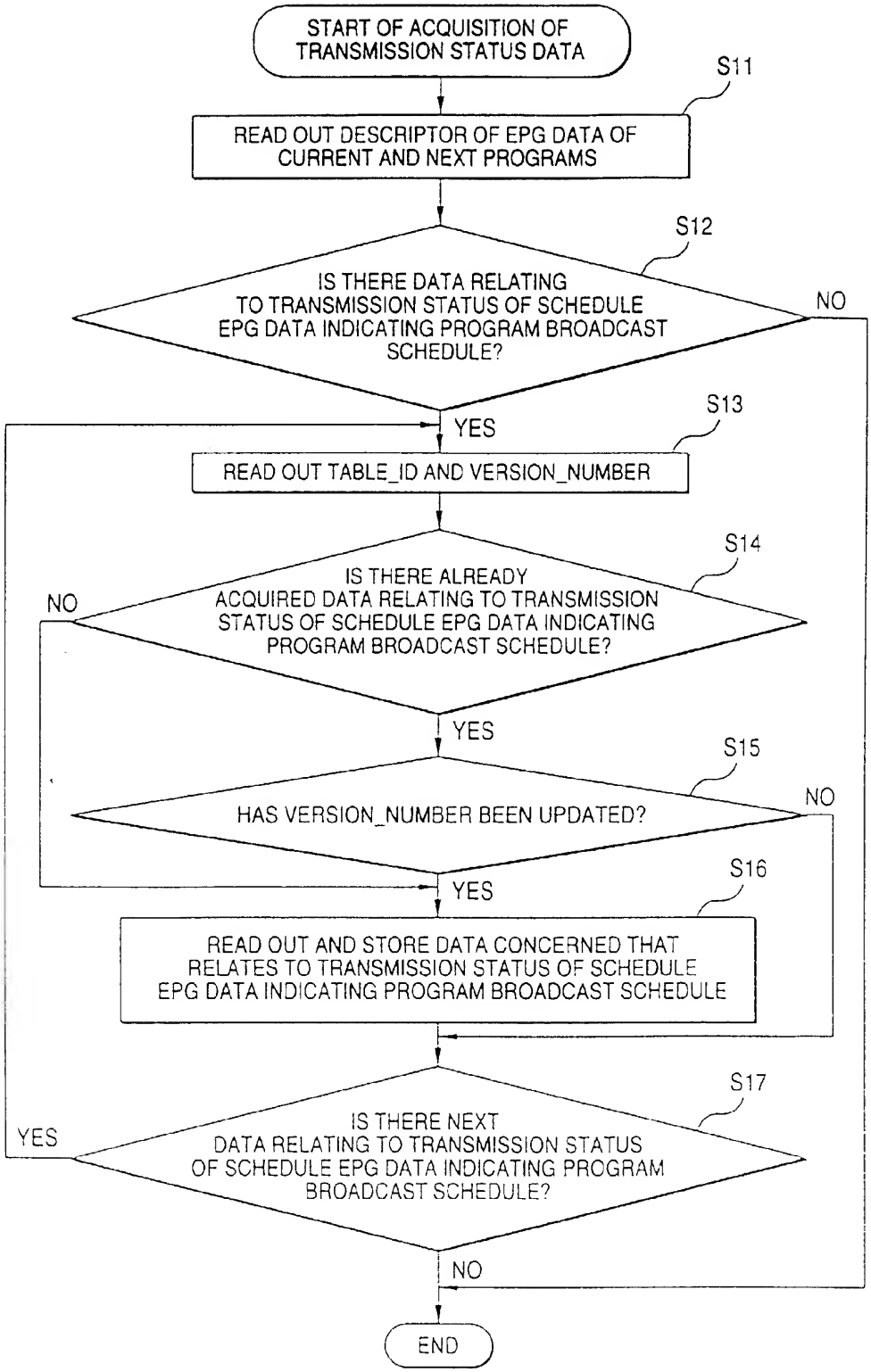
START OF ACQUISITION OF TRANSMISSION STATUS DATA
S11
READ OUT DESCRIPTOR OF EPG DATA OF CURRENT AND NEXT PROGRAMS
S12
IS THERE DATA RELATING TO TRANSMISSION STATUS OF SCHEDULE EPG DATA INDICATING PROGRAM BROADCAST SCHEDULE?
NO
YES
S13
READ OUT TABLE_ID AND VERSION_NUMBER
S14
IS THERE ALREADY ACQUIRED DATA RELATING TO TRANSMISSION STATUS OF SCHEDULE EPG DATA INDICATING PROGRAM BROADCAST SCHEDULE?
NO
YES
S15
HAS VERSION_NUMBER BEEN UPDATED?
NO
YES
S16
READ OUT AND STORE DATA CONCERNED THAT RELATES TO TRANSMISSION STATUS OF SCHEDULE EPG DATA INDICATING PROGRAM BROADCAST SCHEDULE
S17
IS THERE NEXT DATA RELATING TO TRANSMISSION STATUS OF SCHEDULE EPG DATA INDICATING PROGRAM BROADCAST SCHEDULE?
YES
NO
END

FIG. 12

SYNTAX	NUMBER OF BITS	MNEMONIC
table_information_section () {		
table_id	8	uimsbf
section_syntax_indicator	1	bslbf
reserved_future_use	1	bslbf
reserved	2	bslbf
section_length	12	uimsbf
service_id	16	uimsbf
reserved	2	bslbf
version_number	5	uimsbf
current_next_indicator	1	bslbf
section_number	8	uimsbf
last_section_number	8	uimsbf
transport_stream_id	16	uimsbf
original_network_id	16	uimsbf
segment_last_section_number	8	uimsbf
last_table_id	8	uimsbf
for (i=0; i<N; i++) {		
table_id	8	uimsbf
repeating_rate	16	bslbf
update_time	40	bslbf
status_flag	1	bslbf
reserved_future_use	3	bslbf
descriptors_loop_length	12	uimsbf
for (i=0; i<N; i++) {		
descriptor ()		
}		
}		
CRC_32	32	rpchof
}		

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TRANSMISSION AND RECEPTION OF TELEVISION PROGRAMS

Abstract:

A television transmitter transmits addditional information in the form of Web pages along with the television signal. The transmission further includes triggers (71) for selectively invoking said Web pages in synchronism with the program. The triggers include (or refer to) a perceptible signal, e.g. a pictogram or an audible beep. In response to receiving a trigger, a receiver reproduces said perceptible signal without substantially disturbing the television screen. The user is thus timely alerted about additional information related to the television program when viewing it. Then, he may or may not invoke the relevant Web page at his own discretion. To inform the public in advance of the triggers that will be broadcast and to provide easy access to the Web pages at an earlier or later stage, the transmission further includes a table of contents (80) identifying the triggers that are being transmitted during the program. The table of contents itself may be invoked by a trigger (70).

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(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL–5621 BA Eindhoven (NL).

(71) Applicant *(for SE only)*: PHILIPS AB [SE/SE]; Kottbygatan 7, Kista, S–164 85 Stockholm (SE).

(72) Inventors: TEN KATE, Warner, Rudolph, Theophile; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL). MATTHEWS, Peter, George; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL). SCHOENMAKERS, Arnoldus, Fransiscus; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL). CHARMAN, Helen, Louis; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL). DOBBELAAR, Astrid; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL).

(74) Agent: SCHMITZ, Herman, J., R.; Internationaal Octrooibureau B.V., P.O. Box 220, NL–5600 AE Eindhoven (NL).

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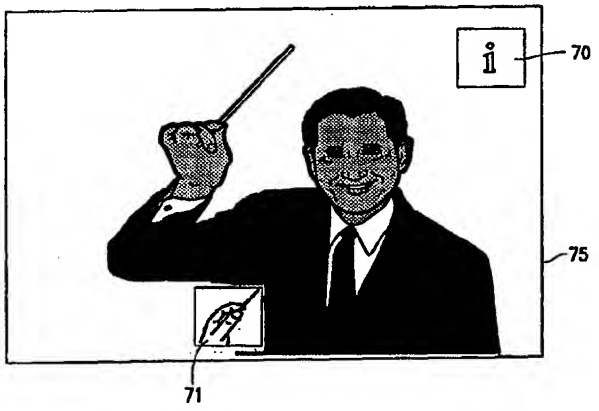

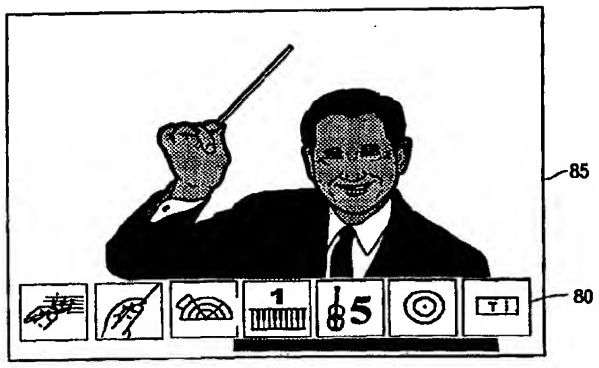

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Transmission and reception of television programs

FIELD OF THE INVENTION

The invention relates to a method of transmitting and receiving television programs. The transmission includes additional information items related to said television programs and trigger data for selectively invoking said information items.

BACKGROUND OF THE INVENTION

A known method as defined in the opening paragraph is disclosed in "Intercast Brings the Web to TV", PC Magazine, January 21, 1997, pp. 203-204. This article describes a method of transmitting Web pages along with a standard television signal. The Web pages provide additional information on what is being broadcast at a particular time. They are downloaded and cached in a receiver's memory. The transmission also includes trigger data (hereinafter also denoted as "triggers") which cause cached pages to be pulled up for display. Said triggers allow the broadcaster to download the pages well in advance and display them at the right moment in the television program. For example, during a commercial for a product, a Web page is pulled up that provides more product information such as available sizes or colors.

The television program, a directory of Web pages, and a selected Web page are displayed in distinct windows of the receiver's display screen. If the television program were displayed in the full screen mode, the user would remain unaware of the Web page that is actually being pulled up. Furthermore, the window showing the directory of Web pages is created by the receiver and necessarily lists only the pages which have already been received.

OBJECT AND SUMMARY OF THE INVENTION

It is an object of the invention to further improve the prior-art system.

To this end, the method according to the invention is characterized in that the trigger data includes a reproducible signal for reproduction by the receiver. This allows the receiver to reproduce said signal upon reception of the trigger and thus to inform the public that additional information about a current event in the program is accessible, even if the television program is being viewed in the full screen mode. Thus the user may or may

not invoke the relevant Web page at his own discretion. The reproducible signal may be a displayable video sub-image, for example, a pictogram. It may also be an audible sound signal, for example, a beep.

An embodiment of the method further comprises the step of transmitting a table of contents identifying the trigger data transmitted during the program. It is thereby achieved that the viewer is informed in advance about the triggers he can expect during the program and to which additional information he will be alerted, even if the information items themselves have not yet been transmitted and received. The table of contents is accessible during the full length of the program. After a trigger has been passed, the viewer may (re)inspect the information still in the context of the television program. Access at a later stage may be along a different path than access during the alerting period in which the trigger is displayed. The table of contents is preferably repetitively transmitted throughout the program in order that it is also available for people who started to watch the program later.

Advantageously, the availability of the table of contents is also signalled to the user by the transmission of an appropriate trigger.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 shows schematically a transmission system comprising a transmitter and a receiver in accordance with the invention.

Fig.2 shows the transmission format of additional information transmitted by the transmitter shown in Fig.1.

Fig.3 shows the transmission format of trigger data transmitted by the transmitter shown in Fig.1.

Fig.4 shows the transmission format of a table of contents transmitted by the transmitter shown in Fig.1.

Fig.5, composed of Figs. 5A and 5B, shows an example of data transmitted along with the television signal during a television program broadcast by the transmitter shown in Fig.1.

Fig.6 shows a flow chart of a program stored in and executed by a microprocessor in the receiver shown in Fig.1.

Fig.7 shows examples of a television screen illustrating the features of the invention.

DESCRIPTION OF EMBODIMENTS

Fig.1 shows schematically a transmission system in accordance with the invention. The system comprises a transmitter **1** and at least one receiver **2** connected together through a channel **3**. The channel **3** may be a broadcast channel, for example, a satellite connection, a terrestrial broadcast network or a cable. As the advantageous effects of the invention are also achieved when playing back a prerecorded program from a storage medium, the channel **3** may also be such a storage medium, for example, a magnetic tape or an optical disc on which the output signal of the transmitter has been recorded. Optionally, a second channel **4** (return channel or bi-directional channel) between the transmitter and the receiver is provided in the form of the Public Switched Telephone Network PSTN or Integrated Service Digital Network ISDN.

The transmitter **1** comprises a television signal source **10** which is shown in the Figure as a studio tape recorder playing back a prerecorded television program. The television signal TV from the source **10** is encoded by an MPEG encoder **11** into a digital MPEG television signal MP. The transmitter further comprises a first storage medium **12** and a second storage medium **13**. The first storage medium **12** stores a number of Web pages W with additional information related to the television program. The second storage medium **13** stores trigger data items T for invoking said Web pages and a table of contents TOC. In practice, both storage media **12** and **13** will be sections of a single hard disk unit. The triggers T and selected ones of the Web pages W are read from the respective storage media in synchronism with the television program under the control of synchronization signals S delivered by the signal source **10**. They are multiplexed with the digital television signal MP by means of a multiplexer **14** into an MPEG Transport Stream TS and transmitted to the receiver **2**. Optionally, the transmitter also comprises an Internet access terminal **15** which enables receivers to access the Web pages W stored in the first storage medium **12** through the Public Switched Telephone Network **4**.

The receiver **2** comprises a demultiplexer **20** which separates the encoded television signal MP from the triggers T, table of contents TOC, and Web pages W. The television signal MP is applied to an MPEG decoder **21** which decodes the audio component A for reproduction by a speaker **22** and the video component V for full-screen display on a display screen **23**. The triggers T, table of contents TOC, and Web pages W are applied to a microprocessor **24** which is arranged to store these types of data in a memory **25** for subsequent processing. The microprocessor is arranged to store selected information in a

predetermined display section of the memory **25**. The data in said display section is converted by a character generator **26** into a displayable graphics signal G which is applied to a combiner stage **27** for display on the screen **25**, solely or in combination with the video signal V. The microprocessor **24** is further connected to a (remote) control unit **28** and, optionally, a modem **29** for accessing the Internet.

Fig.2 shows the transmission format of Web pages W transmitted by the transmitter **1**. A type field **100** identifies the type of information which is the character "W" for Web pages in this example. An address field **101** defines an address (here a file name) by which the pages are retrieved from the broadcast signal and stored in the receiver's memory. Numeral **102** denotes the contents of the page made up in the popular HTML format (HyperText Mark-up Language).

Fig.3 shows the transmission format of the triggers T transmitted by the transmitter. For triggers, the type field **100** is the character "T". A display data field **103** defines (or refers to) a reproducible data signal such as a visual pictogram or an audible signal. The same field can also define how long the signal must be reproduced. A link field **104** defines the location where the Web page to which the trigger is linked can be found. For the purpose of disclosing this invention, the link field **104** has one of two formats. The format http://www.X/Y refers to Web page Y of content provider X on the Internet. The format dvb://X/Y refers to Web page Y which is transmitted along with the television signal transmitted by broadcast station X.

The operation of the system shown in Fig.1 will now be described with reference to an example. In this example, a classical concert is being broadcast. A plurality of Web pages with additional information related to the television program are transmitted during the broadcast for consultation by the user if he so wishes. Some of these pages are transmitted along with the television signal, others can only be accessed through the Internet. The following Web pages with additional information related to the concert are accessible in this example:

- information about the composer to whom the concert is dedicated,
- information about the conductor,
- information about each individual piece of music (Piano concert No.1 and Symphony No.5, respectively, in this example),
- the orchestral layout,
- an order form for purchasing a CD of the concert, and
- an order form for purchasing a ticket for a forthcoming concert.

The broadcaster informs the user about the availability of these Web pages by transmitting respective triggers at adequate points of time during the concert. Upon reception of a trigger, the receiver displays the pictogram or reproduces the audible signal which is defined in the trigger's display data field **103** (see Fig.3). The pictogram is displayed in the (full-screen) television image area. The user may then access the relevant Web pages by simply clicking the pictogram or pressing a dedicated button on the remote control unit. Three types of triggers can be identified:

- Static triggers relate to the television program as a whole.
- Dynamic triggers relate to a current event in the program.
- Living triggers are a combination of a static trigger and a dynamic link. The visualization of the trigger remains unchanged but the actual link field **104** adapts to the action in the program.

The triggers being transmitted and presented during the program are listed together in a table of contents. Fig.4 shows the transmission format of tables of contents. They are identified by the character "TOC" in their type field **100**. The type field is followed by a list of triggers, each comprising a display data field **103** and a link field **104**. In the TOC, the link field **104** may be empty, for example, if the relevant Web page has not yet been broadcast. Upon reception by the receiver, the TOC will be stored at a predetermined memory location, for example, under the reserved file name "toc". An address field similar to the address field **101** shown in Fig.2 can therefore be dispensed with.

In the example of the TOC shown in Fig.4, seven triggers **41-47** are listed which will be transmitted during the classical concert broadcast. Initially, i.e. at the beginning of the program when the TOC is transmitted prior to the transmission of any of the above-mentioned Web pages with program-related additional information, all of the respective link fields **104** refer to Web pages on the Internet. This allows the user to consult the relevant Web pages already at the beginning of the concert if he so wishes. However, as will be explained hereinafter, the TOC is regularly transmitted with updated link fields.

Fig.5 (which is composed of Figs. 5A and 5B) shows the actual data (tables of contents TOC, Web pages W, triggers T) that are transmitted along with the television signal during the classical concert broadcast. Numeral **51** denotes the first transmission of the table of contents. At this stage, all link fields in the TOC refer to Web pages on the Internet as shown in Fig.4. Numeral **52** denotes the transmission of a trigger T enabling the user to access the TOC which has just been received. The link field of this trigger is "toc" which is the reserved file name for the table of contents. The trigger **52** is an example of a static

trigger. The relevant pictogram remains displayed during the whole program, for example, in an upper corner of the television image. Alternatively, the TOC can be accessed by pressing a dedicated information button (**281** in Fig.1) on the remote control unit.

Numeral **53** denotes the transmission, at the beginning of the program (e.g. during announcements), of a Web page with background information about the composer to whom the concert is dedicated. The page is stored in the receiver under the file name "composer". Then, a trigger **54** is transmitted which causes the embedded pictogram to be inserted into the television image for a defined period of time. The user may click the pictogram and cause the composer Web page to be read from the memory and displayed on the screen.

Numeral **55** denotes the transmission of an updated version of the table of contents. The updated TOC differs from the first version in that the link field of the composer trigger (**41** in Fig.4) is changed from an Internet link (http://www.bbc/composer) to a link to the broadcast page (dvb://bbc1/composer). Accordingly, if the user accesses the composer page via the TOC at a later stage, the receiver will acquire the page from the local memory rather than from the Internet, as was the case at the very beginning of the program.

When the first notes of the first piece of music (Piano Concert No.1) are being broadcast, the transmitter transmits a Web page **56** with background information about this piece of music, which is followed by the transmission of a trigger **57**. As long as the relevant pictogram is displayed, the viewer can consult the respective page by simply clicking the pictogram. As is shown in the Figure, the page is stored under the file name "curpiece". Subsequently, the table of contents is updated by transmitting a new TOC **58** in which the link field **104** of trigger **44** (see Fig.4) has been changed from http://www.bbc/piano1 to dvb://bbc1/curpiece.

During the first piece of music, a Web page **59** showing a layout of the orchestra and a Web page **60** with background information about the conductor of the orchestra are transmitted and stored in the receiver. Their transmission is followed by an update **61** of the TOC in which the link field of layout trigger **43** (see Fig.4) has been changed from http://www.bbc/orchlayout to dvb://bbc1/orchlayout, and the link field of conductor trigger **42** (see Fig.4) has been changed from http://www.bbc/conductor to dvb://bbc1/conductor. The triggers T for invoking these Web pages by clicking the relevant pictogram are denoted **62** and **63** in the Figure. They are transmitted at appropriate moments during the program, i.e. during a close-up view of the conductor and a global view of the

orchestra, respectively. Note that the other information items such as the composer page can be accessed at any time via the table of contents. To this end, the user clicks the TOC pictogram or presses the information button and selects a desired pictogram from the table of contents which is displayed in response thereto.

Reference numeral **64** denotes the transmission of a Web page with information about the second piece of music (Symphony No.5). Numeral **65** denotes a trigger for invoking this page which is transmitted when this piece is being played. In this example, the Symphony No.5 page replaces the Piano Concert No.1 page because both pages have the same file name "curpiece". This is not essential but is shown to illustrate the flexibility of the invention. Although the trigger associated with the Piano Concert No.1 will no longer be transmitted, the information remains accessible to the user via the Internet. To this end, the link field of trigger **44** in the table of contents (see Fig.4) is restored to its original value http://www.bbc/piano1 in an updated version **66** of the TOC. While Symphony No.5 is being played, triggers **67** and **68** for invoking the conductor and orchestral layout pages are again transmitted during a close-up view of the conductor and a global view of the orchestra, respectively.

At the end of the program, announcements are made about the possibility to buy a CD of the concert and a ticket for the next concert in the concert hall. During these announcements, triggers **69** and **70** are transmitted. Clicking the corresponding pictogram causes the receiver to establish an Internet connection with a CD shop or the concert hall, respectively, allowing him to order the CD or ticket. Finally, a new TOC **71** is transmitted in which all link fields are given their initial value as shown in Fig.4. After the program has finished, the viewer is thus still kept informed about the program's additional information and he can still access the Web pages via the Internet.

Although the receiver **2** (see Fig.1) has already been described functionally in the above example, its operation will now be described in more detail. The operation of the receiver is determined by a program which is stored in, and executed by, the microprocessor **24**. Fig.6 shows a flow chart illustrating this program. References in this description which are made to various circuit elements of the receiver refer to the schematic diagram shown in Fig.1. In the flow chart, numeral **200** denotes a reset operation which is carried out when the receiver is tuned to a television program. In a step **201**, the microprocessor awaits reception of a data item (W, T, TOC) from the multiplexer **20** or reception of a control command (C)

from the remote control unit **28**. If a data item is received, the program proceeds with step **210**. If a control command is received, the program proceeds with step **220**.

In the step **210**, the microprocessor reads the type field of the received data item. If the type field is "W", the data item is a broadcast Web page. In a step **211**, said page is stored in the receiver's memory **25** under the file name which is included in the address field of the Web page. If the type field is "T", the data item is a trigger. In a step **212**, the microprocessor stores the pictogram embedded in the display data field in the display section of memory **25**. In response thereto, the character generator **26** displays the pictogram as an overlay over the television image. The link field of the trigger is also saved in memory. If the type field is "TOC", the data item is a table of contents. In a step **213**, said table is stored in memory **25** under the file name 'toc". After thus having processed a received data item, the program returns to the step **201** to await further events.

In the step **220**, the microprocessor investigates whether the received control command is a toggle command to switch the display of the table of contents on or off. The relevant command is issued by pressing a special i-button (**281** in Fig.1) of the remote control unit or pointing-and-clicking the i-pictogram in the upper right corner of the television screen. Then a step **221** is executed in which the table of contents is displayed or, if the TOC is already displayed, erased.

Other control commands are point-and-click operations for navigating through the information associated with the television program. In a step **222**, the link field associated with the pictogram being clicked is read. This applies to triggers that have just been received as well as triggers that are listed in the table of contents. In a step **223**, the microprocessor determines whether the link field is filled in and, if this is the case, whether it represents an Internet address (http://..) or a broadcast address (dvb://..). In the table of contents, link fields may initially be empty. In that case, the microprocessor generates an on-screen-display message informing the user that the selected information item will be transmitted and received later during the program. The user is thus informed about information still to come.

If the link field is an Internet address, a step **224** is carried out in which the microprocessor activates modem **29** for establishing an Internet connection with the relevant provider. If the receiver has no modem, the user may be informed that the desired information will possibly be transmitted and received later.

If the link field represents a broadcast address, the microprocessor checks in a step **225** whether a page with the associated file name is stored in the receiver's memory **25**. This will usually be the case, and the microprocessor will transfer the stored page to the display section in a step **226**. If the page is not locally available yet, a step **227** is performed in which the user is given an appropriate message that the page is being looked for in the received television signal. Optionally, the receiver may keep a copy of the initial version of the table of contents (see Fig.4) for offering the user an alternative location of the desired information. As an additional option, the transmitter may transmit for this purpose a special backup version of the table of contents in which all link fields refer to Internet Web pages only. Such an option is very useful for viewers who have tuned to the program at a later stage.

Fig.7 shows an example of television screens during the concert. In screen **75**, the conductor trigger has just been transmitted. The corresponding pictogram **71** is displayed, and the viewer can access more information about the conductor by clicking the pictogram. In the upper right corner, the i-pictogram **70** for accessing the table of contents is displayed. Screen **85** shows the result of pointing and clicking said i-pictogram. It causes the display data fields **80** of the triggers listed in the table of contents to be displayed.

In summary, a television transmitter transmits additional information in the form of Web pages along with the television signal. The transmission further includes triggers (71) for selectively invoking said Web pages in synchronism with the program. The triggers include (or refer to) a perceptible signal, e.g. a pictogram or an audible beep. In response to receiving a trigger, a receiver reproduces said perceptible signal without substantially disturbing the television screen. The user is thus timely alerted about additional information related to the television program when viewing it. Thus, he may or may not invoke the relevant Web page at his own discretion. To inform the public in advance of the triggers that will be broadcast and to provide easy access to the Web pages at an earlier or later stage, the transmission further includes a table of contents (80) identifying the triggers that are being transmitted during the program. The table of contents itself may be invoked by a trigger (70).

Claims

1. A method of transmitting television programs (TV) to at least one receiver, including the steps of transmitting additional information items (W) related to said television programs and trigger data (T) for selectively invoking said information items, characterized in that the trigger data includes a reproducible signal (103) for reproduction by the receiver.

2. A method as claimed in claim 1, wherein the reproducible signal is a displayable video sub-image.

3. A method as claimed in claim 1, wherein the reproducible signal is an audible sound signal.

4. A method as claimed in claim 1, further comprising the step of transmitting a table of contents (TOC) identifying the trigger data being transmitted during the program.

5. A method as claimed in claim 4, wherein the table of contents is repetitively transmitted throughout the television program.

6. A method as claimed in claim 4, including the step of transmitting trigger data for invoking said table of contents.

7. A method of receiving television programs, comprising the steps of receiving and storing additional information items related to said television programs and receiving trigger data for selectively invoking said information items, characterized by reproducing a reproducible signal included in the trigger data upon reception of said trigger data and invoking said information item in response to a predetermined user-operable command.

8. A method as claimed in claim 7, wherein the reproducible signal is a displayable video sub-image, comprising the step of displaying said sub-image within the image area representing the television program.

9. A method as claimed in claim 7, comprising the step of receiving and storing a table of contents identifying the trigger data transmitted during the program, displaying said table of contents and invoking stored information items in response to selecting respective trigger data from said table of contents.

10. A transmitter for transmitting television sprogram to at least one receiver, comprising means for transmitting additional information items related to said television

programs and trigger data for selectively invoking said information items, characterized in that the trigger data includes a reproducible signal for reproduction by the receiver.

11. A transmitter as claimed in claim 10, further comprising means for transmitting a table of contents identifying the trigger data transmitted during the program.

12. A receiver for receiving television programs, comprising means for receiving and storing additional information items related to said television programs and receiving trigger data for selectively invoking said information items, characterized by means for reproducing a reproducible signal included in the trigger data upon reception of said trigger data and invoking said information item in response to a predetermined user-operable command.

13. A receiver as claimed in claim 12, wherein the reproducible signal is a displayable video sub-image, comprising means for displaying said sub-image within the image area representing the television program.

14. A receiver as claimed in claim 12, comprising means for receiving and storing a table of contents identifying the trigger data transmitted during the program, displaying said table of contents and invoking stored information items in response to selecting respective trigger data from said table of contents.

15. A television signal including additional information items related to said television programs and trigger data for selectively invoking said information items, characterized in that the trigger data includes a reproducible signal for reproduction by the receiver.

16. A signal as claimed in claim 15, further including a table of contents identifying the trigger data transmitted during the program.

17. A storage medium on which a television signal as claimed in claim 15 or 16 is stored.

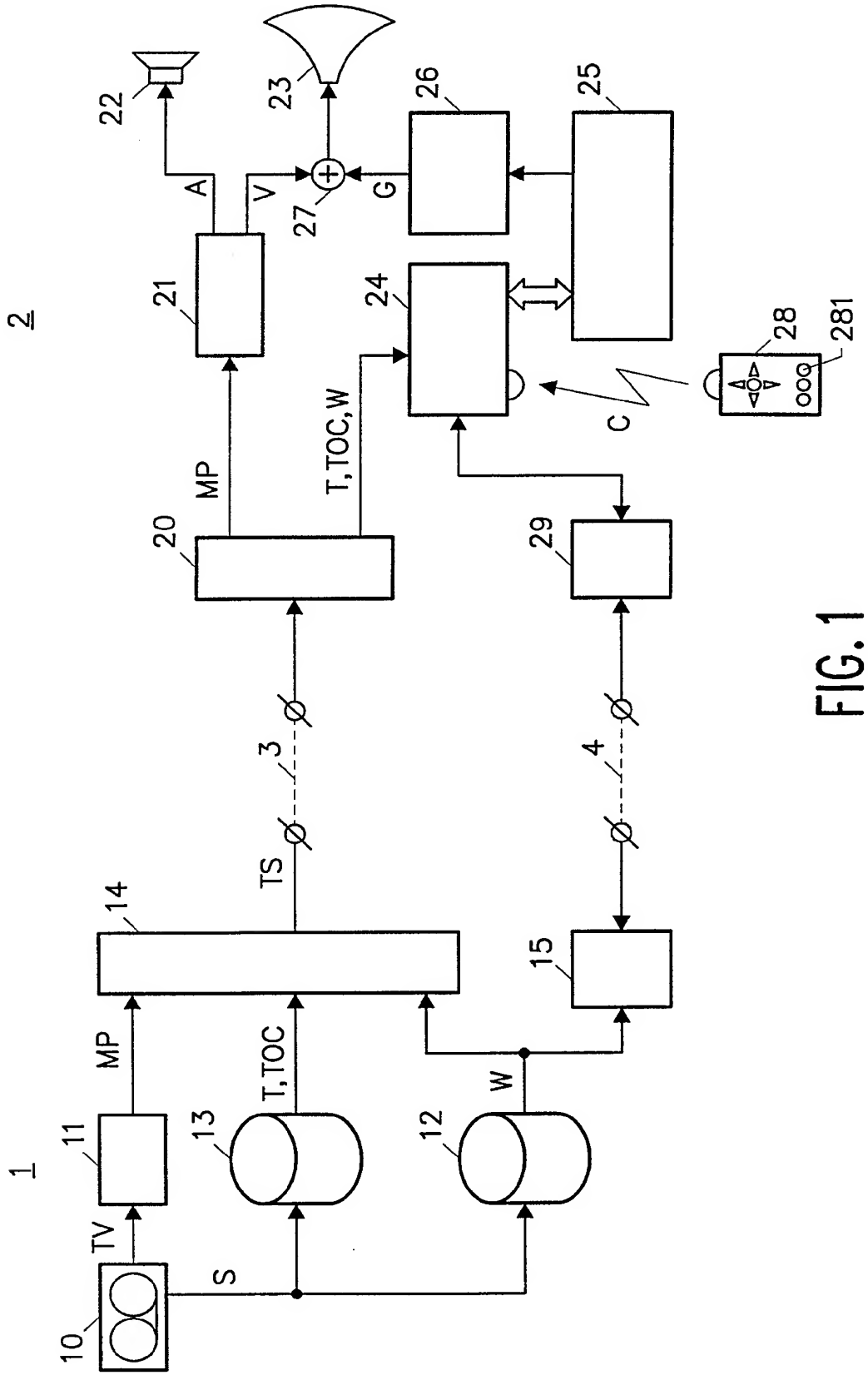
1
2
10
11
12
13
14
15
20
21
22
23
24
25
26
27
28
281
29
TV
S
MP
T,TOC
W
TS
3
4
A
V
G
C
T,TOC,W
MP

FIG. 1

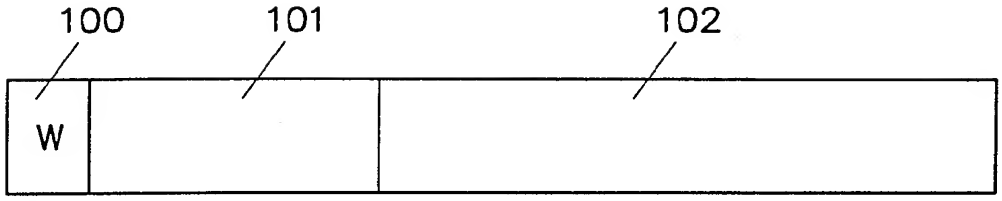

FIG. 2

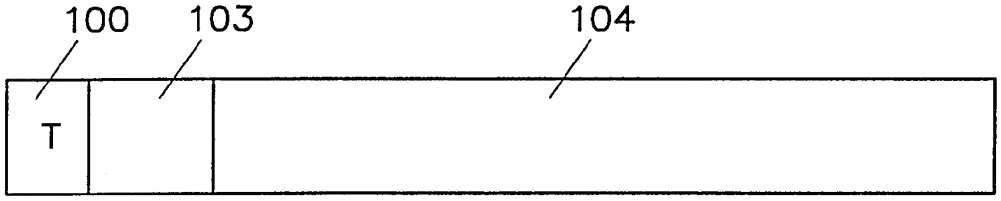

FIG. 3

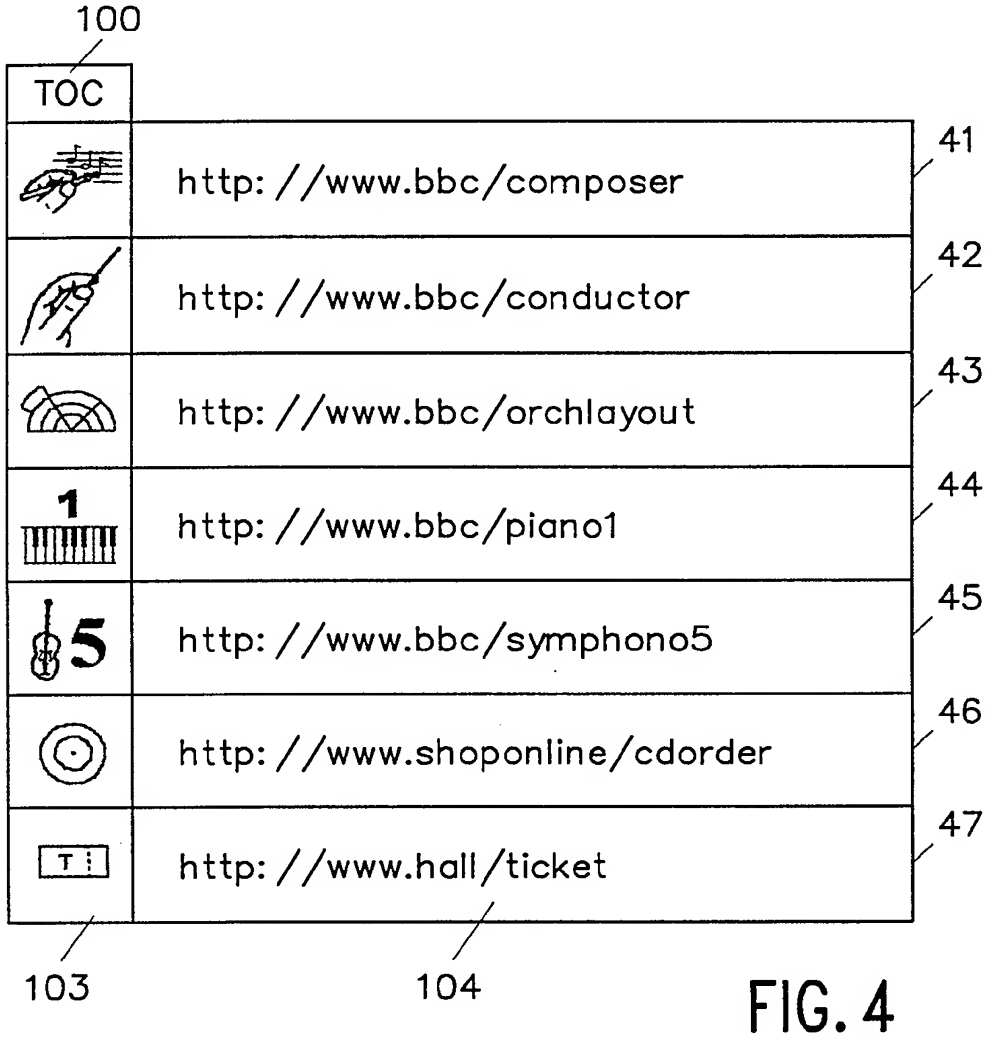

FIG. 4

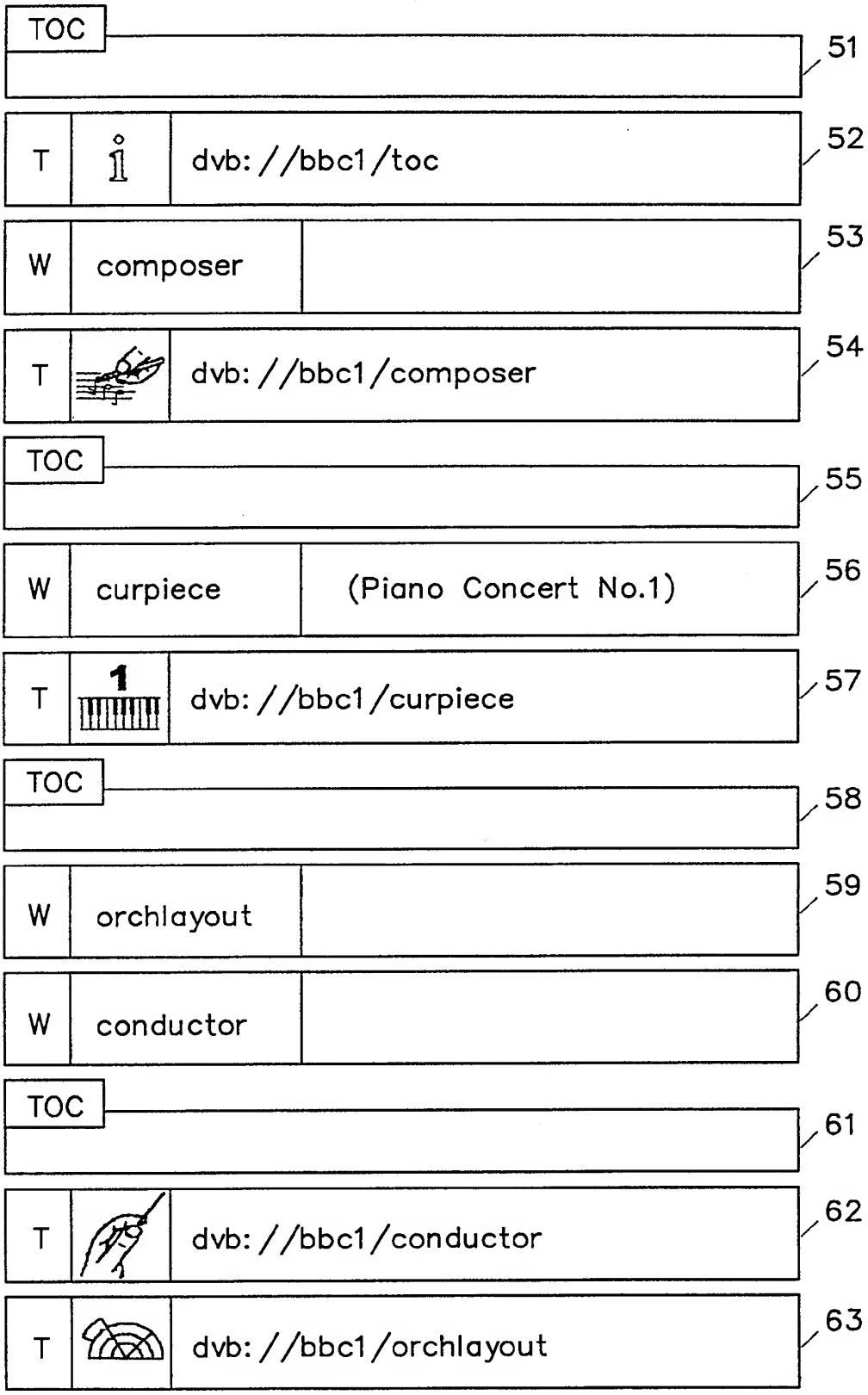
TOC
51
T
dvb://bbc1/toc
52
W
composer
53
T
dvb://bbc1/composer
54
TOC
55
W
curpiece
(Piano Concert No.1)
56
T
1
dvb://bbc1/curpiece
57
TOC
58
W
orchlayout
59
W
conductor
60
TOC
61
T
dvb://bbc1/conductor
62
T
dvb://bbc1/orchlayout
63

FIG. 5A

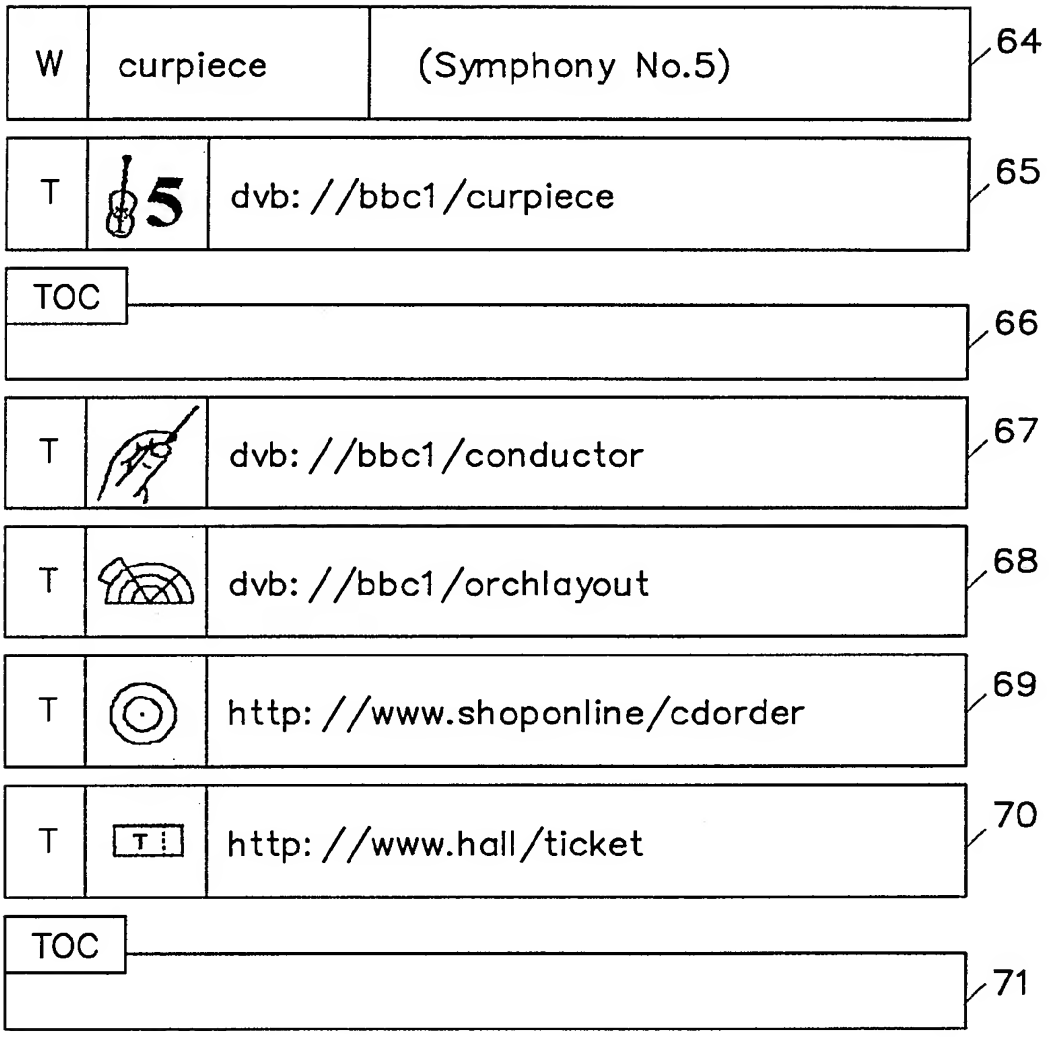
W
curpiece
(Symphony No.5)
64
T
dvb: //bbc1/curpiece
65
TOC
66
T
dvb: //bbc1/conductor
67
T
dvb: //bbc1/orchlayout
68
T
http: //www.shoponline/cdorder
69
T
http: //www.hall/ticket
70
TOC
71

FIG. 5B

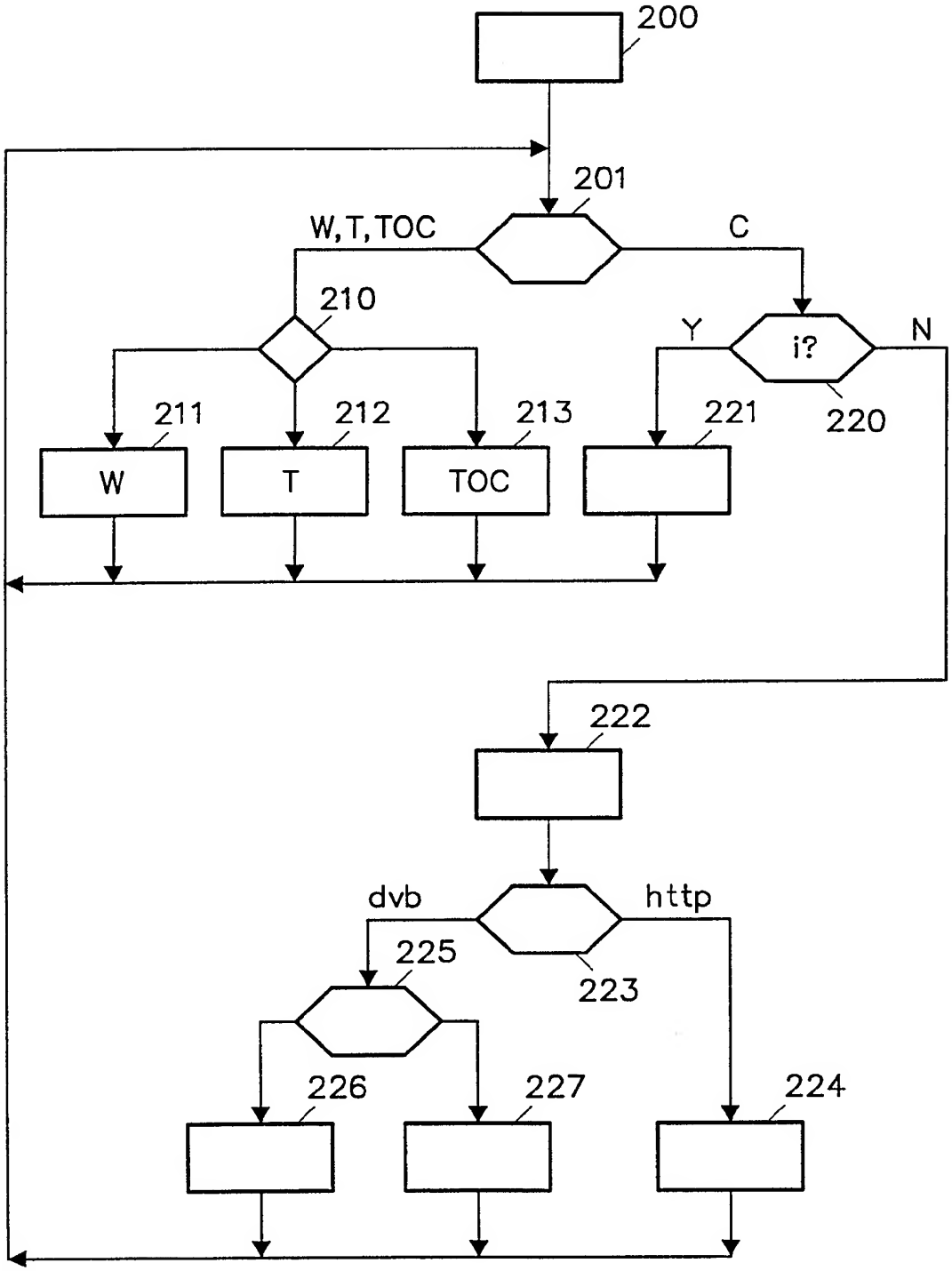
200
201
W,T,TOC
C
210
Y
i?
N
211
212
213
221
220
W
T
TOC
222
dvb
http
225
223
226
227
224

FIG. 6

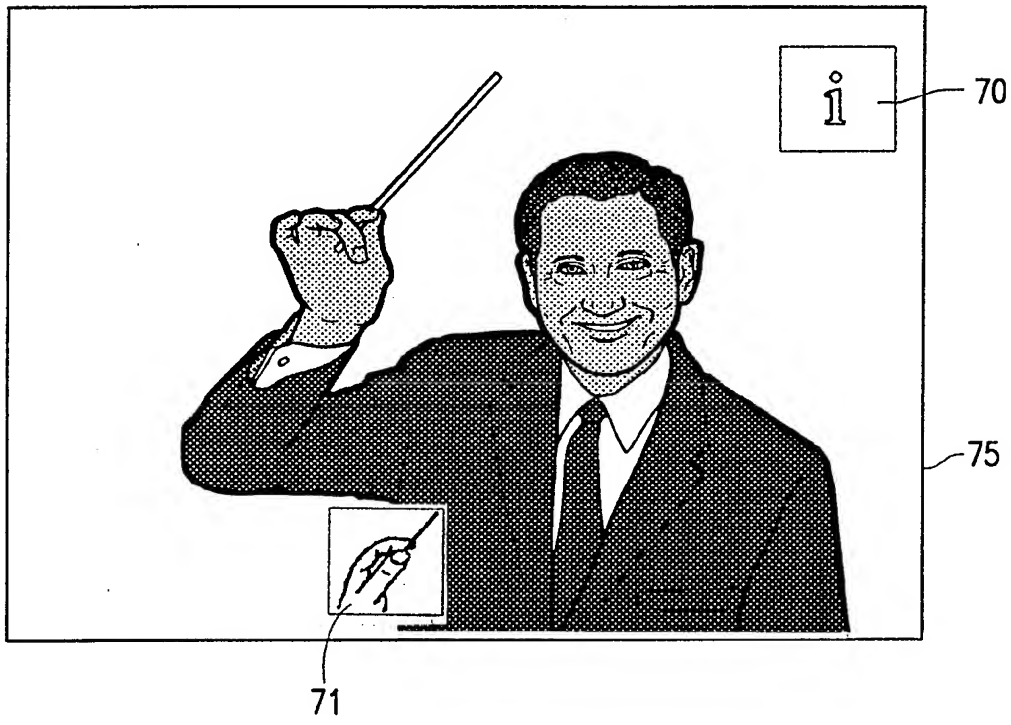

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 98/00580

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04N 7/173, H04N 5/445
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 9641478 A1 (TV GUIDE ON SCREEN), 19 December 1996 (19.12.96), claims 1-5, abstract ---	1-17
A	US 4488179 A (H. ECKHARD KRÜGER ET AL), 11 December 1984 (11.12.84), abstract --- --------	1-17

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" erlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 April 1998	05 -10- 1998
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Rune Bengtsson Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

27/07/98

International application No.
PCT/IB 98/00580

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9641478 A1	19/12/96	AU 6258596 A	30/12/96
		EP 0856227 A	05/08/98
		PL 323914 A	27/04/98
		US 5589892 A	31/12/96
US 4488179 A	11/12/84	DE 3036552 A,C	13/05/82
		JP 1766313 C	11/06/93
		JP 4040912 B	06/07/92
		JP 57087682 A	01/06/82

WO0005890

Publication Title:

METHOD AND APPARATUS FOR ENCODING A USER INTERFACE

Abstract:

Abstract of WO 0005890

(A1) Translate this text A method and apparatus for combining video frame sequences with a video display of an interactive program guide (IPG). The apparatus comprises a plurality of compositors that combine background information, video frame sequences and program guide graphics into a single video frame sequence. The sequence is then digitally encoded to form an MPEG-like bitstream. The same background information and informational video is composited with a different program guide graphic to form another video sequence that is also encoded. A plurality of such sequences are produced with each sequence having a different program guide graphic. Each sequence is encoded and then multiplexed into a transport stream such that all the encoded sequences are transmitted to a subscriber's terminal using a single transport stream. As such, the subscriber can transit from one program guide to the next without interruption of the background or video display as the program guide graphic is changed.

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International Bureau

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(51) International Patent Classification 7 : H04N 7/16

A1

(11) International Publication Number: WO 00/05890

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(30) Priority Data:

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09/201,528	30 November 1998 (30.11.98)	US
09/293,526	15 April 1999 (15.04.99)	US
09/359,561	22 July 1999 (22.07.99)	US

(71) Applicant: DIVA SYSTEMS CORPORATION [US/US]; Building 203, 333 Ravenswood Avenue, Menlo Park, CA 94025 (US).

(72) Inventors: LUDVIG, Edward, A.; 831 Canyon Road, Redwood City, CA 94062 (US). GORDON, Donald, F.; Apartment 10, 465 Gabilan Street, Los Altos, CA 94022 (US). OSBORN, Nathan, W.; 1150 Cloud Avenue, Menlo Park, CA 94025 (US). BAYRAKERI, Sadik; 733 Shell Boulevard #104, Foster City, CA 94404 (US).

(74) Agent: MOSER, Raymond, R.; Thomason, Moser and Patterson, 2 Bridge Avenue, P.O. Box 8160, Red Bank, NJ 07701 (US).

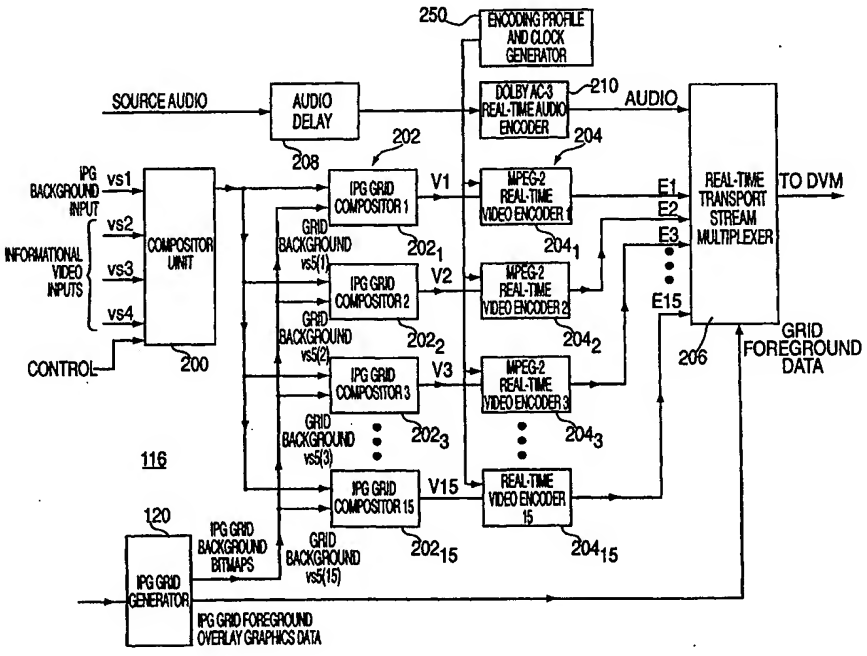
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: METHOD AND APPARATUS FOR ENCODING A USER INTERFACE

(57) Abstract

A method and apparatus for combining video frame sequences with a video display of an interactive program guide (IPG). The apparatus comprises a plurality of compositors that combine background information, video frame sequences and program guide graphics into a single video frame sequence. The sequence is then digitally encoded to form an MPEG–like bitstream. The same background information and informational video is composited with a different program guide graphic to form another video sequence that is also encoded. A plurality of such sequences are produced with each sequence having a different program guide graphic. Each sequence is encoded and then multiplexed into a transport stream such that all the encoded sequences are transmitted to a subscriber's terminal using a single transport stream. As such, the subscriber can transit from one program guide to the next without interruption of the background or video display as the program guide graphic is changed.



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METHOD AND APPARATUS FOR ENCODING A USER INTERFACE

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of U.S. provisional patent application serial number 60/093,891 filed July 23, 1998 which is hereby incorporated herein by reference. This application is also a continuation-in-part of commonly assigned U.S. Patent Application serial number 09/293,526 filed April 15, 1999 and commonly assigned U.S. Patent Application serial number 09/201,528 filed November 30, 1998, both of which are hereby incorporated herein by reference.

BACKGROUND OF THE DISCLOSURE

1. Field of the Invention

The invention relates to electronic program guides and, more particularly, the invention relates to a technique for encoding a user interface of an information distribution system.

2. Description of the Background Art

In several communications systems, the data to be transmitted is compressed so that the available transmission bandwidth is used more efficiently. For example, the Moving Pictures Experts Group (MPEG) has promulgated several standards relating to digital data delivery systems. The first, known as MPEG-1 refers to ISO/IEC standards 11172 and is incorporated herein by reference. The second, known as MPEG-2, refers to ISO/IEC standards 13818 and is also incorporated herein by reference. A compressed digital video system is described in the Advanced Television Systems Committee (ATSC) digital television standard document A/53, and is incorporated herein by reference.

The above-referenced standards describe data processing and manipulation techniques that are well suited

to the compression and delivery of video, audio and other information using fixed or variable rate digital communications systems. In particular, the above-referenced standards, and other "MPEG-like" standards and techniques, compress, illustratively, video information using intra-frame coding techniques (such as run-length coding, Huffman coding and the like) and inter-frame coding techniques (such as forward and backward predictive coding, motion compensation and the like). Specifically, in the case of video processing systems, MPEG and MPEG-like video processing systems are characterized by prediction-based compression encoding of video frames with or without intra- and/or inter-frame motion compensation encoding.

Over the past few years, television has seen a transformation in a variety of means by which its programming is distributed to consumers. Cable television systems are doubling or even tripling system bandwidth with the migration to hybrid fiber coax (HFC) cable plant thereby offering a larger number of channels to the viewer. Customers unsatisfied with their local cable systems have switched in high numbers to direct broadcast satellite (DBS) systems. And, a variety of other approaches have been attempted focusing primarily on high bandwidth digital technologies, intelligent two way set top boxes, or other methods of trying to offer service differentiated from standard cable and over the air broadcast systems.

With this increase in bandwidth, the number of programming choices has also increased. Leveraging off the availability of more intelligent set top boxes, several companies such as Starsight and Prevue Guide have developed elaborate systems for providing an interactive listing of a vast array of channel offerings, expanded textual information about individual programs, the ability to look forward to plan television viewing as much as several weeks in advance, and the option of automatically programming a VCR to record a future broadcast of a television program.

Unfortunately, the existing program guides have several drawbacks. They tend to require a lot of memory, some of

them needing upwards of one megabyte of set top terminal (STT) memory. They are very slow to acquire their current database when they are activated for the first time or are subsequently restarted (e.g., a large database may be downloaded to a STT using only a vertical blanking interval (VBI) data insertion technique). Disadvantageously, such slow database acquisition may result in out of date database information or, in the case of a pay per view (PPV) or video-on-demand (VOD) system, limited scheduling flexibility for the information provider. The user interface to existing program guides does not usually look like a typical television control interface; rather looks like a 1980's style computer display (i.e., blocky, ill-formed text and/or graphics).

Additionally, the present program guides may provide an advertising or preview region along with the program guide graphics. However, the insertion of these additional video signals is performed using an analog compositor that merely inserts (overlays) the additional imagery into the broadcast stream. The analog compositing process is accomplished and then the new analog video containing an advertisement or preview and the program guide are recorded on tape for subsequent broadcast. This compositing process is not accomplished in real time at the head end of the cable system and, consequently, the program guide can not contain targeted advertising for a particular household or a particular neighborhood or region. The program guide with its associated preview or advertising is broadcast to all subscribers connected to the head end of the cable system. Additionally, these program guides are generally passive, in that, the viewer sees the program guide information change on the screen to indicate different programs and their associated channels. However, there is no provision enabling a viewer to interact with the program guide display to scroll through the channel or channels that are available. Because such scrolling in an analog system requires a splice to a new program guide video sequence, the program guides that are interactive do not include

advertising video or other video information with the program guide.

Therefore, it is desirable to provide a method and apparatus for encoding an interactive program guide.

SUMMARY OF THE INVENTION

The disadvantages associated with the prior art are overcome by the present invention of a method and apparatus for encoding user interface of an information distribution system. One embodiment of such user interface is an interactive program guide (IPG) that forms an IPG screen or page containing a graphical guide region and a video region playing at least one video sequence. The invention is a method and apparatus for performing ensemble encoding of one or more IPG pages. The invention comprises a plurality of compositors that combine background information, informational video and program guide graphics into a single sequence of video frames. The sequence is then digitally encoded to form an MPEG-like bitstream. The same background information and informational video is composited with a different program guide graphic to form another video sequence that is also encoded. A plurality of such bitstreams are produced with each sequence containing a different program guide graphic. The encoding is performed using a common coding profile and a common clock for each of the encoders. The encoded sequences are then multiplexed into at least one transport stream such that all the encoded sequences are transmitted to subscriber equipment using one or more transport streams. As such, the subscriber can transition from one program guide page to the next without interruption of the background or informational video as the program guide page graphic is changed.

The informational video may appear in multiple locations upon the IPG screen. Promotional or advertising video may appear in one portion while an animated graphic appears in another location. Each of the informational video streams may have a different rate of display. The

encoders handle different video rates by using slice based encoding of the composite image sequence.

One example of a program guide that is encoded in accordance with the invention has each graphic containing a set of programs (e.g., channels) listed along a left, vertical axis and each program associated with the channel is identified in a rectangular cell that extends toward the right. The horizontal axis represents time and about 1.5 hour of programming for ten channels is shown in each program guide graphic page. The informational video is generally contained in one or more regions above the program graphic.

In another example of a program guide that is encoded in accordance with the invention has each graphic containing a set of programs (e.g., channels) listed along a left, vertical axis and each program associated with the channel is identified in a cell that is listed beneath a time axis. The horizontal axis represents time and about 1.5 hours of programming for eight channels is shown in each program guide graphic page. Each channel is associated with text that represents three programming slots, one for each half hour in the time axis. The informational video is generally contained in one or more regions next to the program graphic, i.e., a guide region is on the left half of the screen and the video region is on the right half of the screen or vice versa.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a high-level block diagram of an information distribution system that uses the interactive program guide of the present invention;

FIG. 2 depicts a block diagram of an IPG generator of the present invention;

FIG. 3 depicts a block diagram of a compositor unit that produces background/informational frame sequence in accordance with the present invention;

FIG. 4 depicts a block diagram of an IPG compositor that inserts an IPG graphic into the background/informational frame sequence;

FIG. 5A-5C depicts a series of illustrative IPG pages;

FIG. 6 depicts another example of an IPG page that can be produced by the invention; and

FIG. 7 depicts a PID map for a set of IPG pages encoded by the invention.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

FIG. 1 depicts a high-level block diagram of an information distribution system 100, e.g., a video-on-demand system or digital cable system, that incorporates the present invention. The system 100 contains service provider equipment (SPE) 102 (e.g., a head end), a distribution network 104 (e.g., hybrid fiber-coax network) and subscriber equipment (SE) 106. This form of information distribution system is disclosed in commonly assigned U.S. patent application serial number 08/984,710 filed December 3, 1997. The system is known as the OnSet™ system provided by DIVA Systems Corporation of Menlo Park, California.

In general, the SPE 102 produces a plurality of digital bitstreams that contain encoded information (e.g., television programming in an MPEG-like compressed form). These bitstreams are modulated using a modulation format that is compatible with the distribution network 104. The subscriber equipment 106, at each subscriber location 106_1, 106_2, ..., 106_n, comprises a demodulator/decoder 124 and a display 126. Upon receiving a bitstream, the subscriber equipment decoder 124 extracts the information from the

received signal and decodes the stream to produce the information on the display, i.e., produce a television program or program guide page.

In an interactive information distribution system such as the one described in commonly assigned U.S. patent application 08/984,710, filed December 3, 1997, the program bitstreams are addressed to particular subscriber equipment locations that requested the information through an interactive menu. An appropriate interactive menu structure for requesting video on demand is disclosed in commonly assigned U.S. patent application serial number 08/984,427, filed December 3, 1997.

To assist a subscriber (or other viewer) in selecting programming, the SPE 102 produces a interactive program guide (IPG) in accordance with the present invention. The IPG of the present invention contains program information, e.g., title, time, channel, program duration and the like, as well at least one region displaying full motion video, i.e., a television advertisement or promotion. Such informational video is provided in various locations within the program guide screen.

FIG. 5A illustrates a first example of an IPG 500 that is produced in accordance with the present invention. The IPG 500 contains a background 502, a plurality of video display regions 504, 506, and 508, and a program guide graphic 510. The program guide graphic 510 contains a left (or right), vertical axis 512 representing the available channels and a bottom (or top), horizontal axis 514 represents time. Generally, about 1.5 to 2 hours of programming are displayed in the guide graphic 510. Each program (e.g., P1, P2, P3, and so on) is identified by a program title within a rectangular cell. The extent of the cell (its length) indicates the duration of the program and the starting location of the left edge of the cell indicates the starting time of the program. The arrangement of the program identification cells in this manner is a conventional arrangement in which programming guides have been organized in print for years.

Returning to FIG. 1, the invention produces the IPG (500 of FIG. 5A) using a novel compositing technique that enables full motion video to be positioned within an IPG and have the video seamlessly transition from one IPG page to another. FIG. 1 depicts the components that are necessary to produce an IPG page that contains at least one video region. The embodiment of the invention is described as having advertising displayed in the video region or regions. However, advertising is merely illustrative of a type of informational video and any sequence of video or graphic information can be displayed in these regions. To this end, the SPE 102 contains a video storage device 108, an informational video selection and monitoring system 110, an IPG generator 116 (an ensemble encoder), a background storage device 118, a controller 114, an IPG grid generator 120, and a digital video modulator 122. The video selection and monitoring system 110 controls timing of the informational video display and, if the video is an advertisement, tracks video utilization to facilitate billing to an advertiser whenever a particular advertisement is transmitted. Thus, the video selection and monitoring system 110 requests that the storage device 108 (e.g., a disk drive or magneto-optical drive) recall and send to the IPG generator 116 a particular video sequence. The video is stored in the storage device 108 as frame-based digital video (i.e., 601 format video) and associated audio. Alternatively, compressed or uncompressed analog video as well as other formats of video information may be stored in the storage device 108. These formats are converted to 601 format prior to sending the video to the IPG generator 116.

As the video is recalled from device 108, each video sequence is coupled to the IPG generator 116. As such, three video streams and one audio stream (e.g., an audio stream associated with one of the advertisements) are provided to the IPG generator 116. Additionally, a background image is recalled from the storage device 118 under instructions from the controller 114. The background image is generally a static graphic, but it may be a video

frame sequence containing moving imagery. Lastly, the IPG grid generator 120 provides a program guide graphic to the IPG generator 116. The IPG data for the graphic can be provided from any one of a number of sources such as a network cable feed, an internet site, a satellite feed, and the like. The guide program data is formatted, for example, into the rectangular grid graphic of program cells (screen 500 of FIG. 5A) by the IPG grid generator 120. As shall be discussed below with respect to FIG. 6, other IPG page layouts may be used and are considered to be within the scope of this invention.

The IPG generator 116 performs ensemble encoding by combining the three video sequences, the background and the guide graphics into a comprehensive IPG display such as the one depicted as IPG page 500 in FIG. 5A or IPG page 600 in FIG. 6. As shall be described in detail below, the informational video is overlaid onto the background to form a background/video composite and then various IPG grids are overlaid upon the background/video composite. In this manner, a number of IPG "pages", for example, fifteen of them, are produced, where each page depicts ten channels of programming information. Each of these IPG pages is encoded within the IPG generator 116 into a compressed digital bitstream, e.g., an MPEG compliant bitstream. The bitstream is then modulated by the digital video modulator 122 using a modulation format that is compatible with the distribution network 104. For example, in the OnSet™ system the modulation is quadrature amplitude modulation (QAM); however, other modulation formats could be used.

The subscriber equipment 106 contains a demodulator/decoder 124 and a display 126 (e.g., a television). The demodulator/decoder 124 demodulates the signals carried by the distribution network 104 and decodes the demodulated signals to extract the IPG pages from the bitstream. As shall be described below, each of the IPG pages is identified with a unique program identification code (known as a PID) that is used by the demodulator/decoder 124 to select a bitstream for decoding.

The decoded IPG page is displayed, as shown in FIG. 5A, to the subscriber or viewer. As the viewer selects another IPG page containing other program information, generally by scrolling to the bottom of the IPG graphic 510 using a remote control interface 128 or some other input device, the IPG page stream associated with the next PID is decoded. The only change the viewer sees is the IPG graphic changes (from, for example, graphic 510_1 to 510_2), the informational video and its associated audio seamlessly continues playing. This seamless play occurs because each of the IPG pages contains the same, frame synchronized background and informational video and only the IPG graphic changes from page to page. As such, the decoder seamlessly transitions from one IPG page to another.

FIG. 2 depicts a block diagram of the IPG generator 116. The IPG generator 116 contains a compositor unit 200, a plurality of IPG grid compositors 202, a plurality of video encoders 204 (e.g., MPEG-2 compliant encoders), a common profile and clock generator 250, a transport stream multiplexer 206, an audio delay 208, an audio encoder 210 (e.g., an Dolby AC-3 audio encoder) and the IPG grid generator 120. The compositor unit 200 positions the informational video sequences (vs2, vs3, vs4) upon the background video imagery (vs1). To facilitate positioning, the controller (114 in FIG. 1) provides the compositor unit 200 with the coordinates of one corner of each informational video and provides a size indicator for each rectangular region in which the video will be displayed relative to the background. The compositor unit 200 performs the placement and fusing of the imagery to form background/information video frame sequence. Further detail of this compositing process is provided below with respect to FIG. 3.

The composite image (e.g., three, full motion video frame sequences positioned upon a background image, the background/informational video) is coupled to a plurality of IPG grid compositors 202_1, 202_2, 202_3, ..., 202_{15} (collectively referred to as compositors 202). The compositors 202 combine the respective IPG graphics with the

background/informational video combination to produce a plurality of video frame sequences containing a composite of the background, the informational video, and the IPG graphics. There is one frame sequence for each IPG graphic, e.g., fifteen sequences in all. As discussed previously, the IPG graphic is produced by the IPG grid generator 120. The IPG grid generator 120 actually produces two items, one is the IPG grid background image (the IPG grid graphic discussed above and shown as graphic 510 in FIG. 5A), and IPG grid foreground overlay graphic data that is used to generate highlighting and other special effects in the displayed IPG screen. Additionally, this data attributes functionality to the highlighted elements such as selecting another IPG page, selecting a program to view, exiting the system, and the like. These special effects and functionality are discussed below with respect to FIGS. 5A, 5B and 5C.

Each of the frame sequences (IPG screen sequences V1, V2, V3, ..., V15) are coupled from the compositors 202 to the plurality of video encoders, e.g., real time MPEG-2 encoders 204_1, 204_2, 204_3, ... 204_n (collectively encoders 204). Each encoder 204 encodes an IPG screen sequence to form a compressed video bitstream, e.g., an MPEG-2 compliant bitstream. The encoders use a common encoding profile and common clock supplied by the encoding profile and clock generator 250. As such, each sequence of IPG frames are synchronously encoded in the same manner.

The IPG grid foreground overlay graphics data is also coupled to the multiplexer 206 from the IPG grid generator 120. This graphics data is generally sent as "user data" or "private data" within the transport stream. Further discussion of the graphics data is provided below.

If the informational video in each IPG page have differing amounts of motion, the encoders can encode the video in a slice-based manner. As such, each frame is divided into a plurality of horizontal stripes of macroblocks. Each frame contains stripe start and stop

identifiers. The information (pixels and/or macroblocks) between the start and stop indentifiers can be encoded in a different manner than other portions of a given stripe. Consequently, a two dimensional region comprising portions of adjacent stripes can be encoded differently from other portions of the frame. The encoded information from the two dimensional region forms a bitstream that is identified by its own program identifier. At the subscriber equipment, the demodulator/decoder decodes the information in each slice, then reassembles the frame by placing the decoded slices into appropriate locations as identified by the slice start/stop identifiers. The two dimensional regions can be specified to align with the informational video such that the regions can contain video having different motion, i.e., fast versus slow motion. Consequently, one region could contain a slow moving animated character while another region could contain a fast moving sporting event promotion and both regions would be coded and decoded accurately.

All the compressed video streams (E1, E2, E3, ..., E15) containing program guide information are multiplexed into a transport stream using multiplexer 206. These compressed video streams may contain the stripe-based encoded streams as well. In addition to the video information, audio information associated with one of the informational videos is also encoded and supplied to the multiplexer 206. The audio signal is delayed in audio delay 208, then encoded in the audio encoder 210. The delay compensates for the time required to perform video encoding of the associated video vis-a-vis the audio encoding. The compressed audio data is coupled to the multiplexer 206 for incorporation into the transport stream.

A transport stream, as defined in ISO standard 13818-1 (commonly known as the MPEG-2 Systems specification), is a sequence of equal sized packets, each 188 bytes in length. Each packet has a 4-byte header and 184 bytes of data. The header contains a number of fields, including packet identification number (PID). The PID field contains 13 bits and uniquely identifies each packet that contains a portion

of a "stream" of video information as well as audio information and data. As such, to decode a particular video bitstream (or audio bitstream or data) for viewing, the decoder in the subscriber equipment extracts packets containing a particular PID and decodes those packets to create the video (and audio) for viewing.

Each of the fifteen bitstreams representing the IPG page sequences within a particular transport stream are uniquely identified by a PID. In the preferred embodiment, fifteen PID's are multiplexed into a single transport stream. Certainly, less of more IPG bitstreams can be included in a transport stream as bandwidth permits. Additionally, more than one transport stream can be used to transmit the IPG bitstreams. For example, additional IPG pages may be encoded that represent additional time within a day or additional channels. The bitstreams representing the additional IPG pages are transmitted in additional transport streams. As such, many IPG pages representing 24 hours of programming on hundreds of channels can be broadcast to the subscriber equipment for selective display to a viewer.

FIG. 7 depicts a graphical representation of PID assignment to each IPG page. The graph 700 contains a PID axis 702 and a time axis 704. At time 1 (t1) and, more than likely, within a single transport stream, the graphics 706 for a first IPG page and the video 708 for a first IPG page are sent in PID1. Then, in PID2, the graphics 710 for a second IPG page and the video 708 for the second IPG page are sent. Note that the video is the same in each IPG page that is sent at time 1 and only the graphics (g_1, $g_2 \ldots g_{15}$) change from IPG page to IPG page. The change in graphics may represent either different time intervals or different channel groupings shown in the IPG pages. In time 2, the grouping and encoding is repeated using different video. The process is repeated until all the IPG pages are generated to cover all available channels over a 24 hour period. The transport streams carrying the encoded IPG pages are then broadcast to all viewers.

An exemplary transport stream consists of N programs multiplexed together into one transport stream. Each program has it's own video PID, which contains all the MPEG bits for a single guide page. All the programs share the same audio and PCR.

To change pages in the guide, it is required to switch between programs (video PIDs) in a seamless manner. This cannot be done cleanly using a standard channel change by the STT switching from PID to PID directly, because such an operation flushes the video and audio buffers and typically gives half a second blank screen.

To have seamless decoder switching, a splice countdown (or random access indicator) method is employed at the end of each video sequence to indicate the point at which the video should be switched from one PID to another.

Using the same profile and constant bit rate coding for each encoding unit, the generated streams for different IPG pages are formed in a similar length compared to each other. This is due to the fact that the source material is almost identical differing only in the characters in the guide from one page to another. In this way, while streams are generated in close lengths, they are not exactly the same lengths. For example, for any give sequence of 15 video frames, the number of transport packets in the sequence varies from one guide page to another. Thus a finer adjustment is required to synchronize the beginnings and ends of each sequence across all guide pages in order for the countdown switching to work.

The invention provides the act of synchronization of a plurality of streams that provides seamless switching at the STT.

Three methods are provided for that purpose:

First, for each sequence you can count the longest guide page for that particular sequence, and then add sufficient null packets to the end of each other guide page so that all the guide pages become the same lengths. Then add the switching packets at the end of the sequence, after all the null packets.

The second method requires buffering of all the packets for all guide pages for each sequence. If this is allowed in the considered system, then the packets can be ordered in the transport stream such that the packets for each guide page appear at slightly higher or lower frequencies, so that they all finish at the same point. Then the switching packets are added at the end of each stream without the null padding.

A third method is to start each sequence together, and then wait until all the packets for all the guide pages have been generated. Once the generation of all packets is completed, switching packets are placed in the streams at the same time and point in each stream.

Depending on the implementation of STT decoder units and requirements of the considered application, each one of the methods can be applied with advantages. For example, the first method, which is null-padding, can be applied to avoid bursts of N packets of the same PID into a decoder's video buffer faster than the MPEG specified rate (e.g., 1.5 Mbit).

The same principles of splicing and synchronization techniques are applicable to a plurality of different transport stream forms, including recombinant stream.

The teachings of the above three methods can be extended apply to similar synchronization problems and to derive similar methods.

Returning to FIG. 1, the transport stream is coupled to a digital video modulator 126 where it is modulated onto a carrier that is appropriate for transmission through the distribution network 104. For a hybrid fiber coax based distribution network 104, the modulation is quadrature amplitude modulation (QAM).

The subscriber equipment 106 is connected to the network 104 and receives the transport stream from the network 104. A demodulator/decoder 124 in each of the terminals extracts the transport stream from the modulation, demultiplexes the bitstreams within the transport stream, and decodes a selected program guide video sequence. Since

the program guide bitstreams are contained in the transport stream, the terminal selects a particular program guide using its unique packet identifier (PID) that causes a video demodulator/decoder 124 to decode the program guide bitstream identified by that PID (or PIDs in the case of slice based encoding). When the user selects another program guide, another stream is decoded based upon the newly selected PID or PIDs. By transmitting many program guide streams in a common transport stream and by frame locking the program guide source, encoding and decoding processes, the latency experienced as a subscriber selects one guide page after another is undetectable. Also, because the informational video is the same and frame synchronized in each program guide bitstream with the only difference being a different guide graphic, the subscriber sees a transition in the guide graphic, but the informational audio and video is seamlessly presented to the viewer.

FIG. 3 depicts a detailed block diagram of the compositor unit 200. The compositor unit 200 contains a plurality of serial-to-parallel converter modules 300 and 304, a plurality of image compositors 302, 306, and 308, an optional parallel-to-serial converter module 310 and a PCI bus 312. The informational video signals vs2, vs3, vs4 are assumed to be supplied as a conventional pixilated video signal in a 601 format (digital video) having each frame of 601 video synchronized with the frames of the other advertisement video signals. Generally, 601 video is supplied as a serial bitstream that is converted into parallel stream, i.e., one complete video frame is coupled to the compositor at a time.

More specifically, the background imagery vs1 and the first informational video vs2 are coupled to the serial-to-parallel converter module 300. The frames of each of these video signals are then coupled to the compositor 302. In operation, the compositor 302 synchronizes the frames, resizes the informational video to fit into a predefined rectangular region, positions the rectangular region on the background and merges the two video frame sequences. The

controller 114 of FIG. 1 uses the PCI bus 312 to instruct the compositor as to the size of the informational video region and its position on the background. A commercially available compositor is used to perform the foregoing operations using 601 video signals.

The composited video sequence containing the background and first informational video is then coupled to the second compositor 306 such that the second informational video is composited onto the background and first video. The third compositor 308 performs a similar function to produce a frame sequence having the background and three informational video sequences composited into a single sequence. The size and position of the informational video display regions is controlled by signals from the controller via the PCI bus 312. The output sequence from the third compositor 308 is optionally coupled to the parallel-to-serial converter module 310 to produce a serial bitstream. Generally, the parallel data is coupled directly to the IPG grid compositors (202 in FIG. 2); however, if the compositor unit 200 is not physically near the compositors 202, then the parallel-to-serial converter 310 may be used to improve the integrity of the data as it is communicated over a distance. Although only three informational videos were added to the background using three compositors, clearly more compositors can be used if additional informational video sequences are desired.

FIG. 4 depicts a block diagram of one of the IPG grid compositors 202, e.g., compositor 202_1. The compositor 202_1 contains an alpha framestore 400, a video framestore 402 and a compositor 406. The alpha framestore 402 stores a bitmap array of weighting functions that control the degree of transparency that the IPG grid will have with respect to the background/informational frame sequence, i.e., the bitmap contains a value of transparency for each and every pixel in the IPG graphic. As such, the alpha framestore information controls the amount of background/advertising video scene that can be viewed "through" the IPG graphic. The video frame store 402 buffers the IPG graphic on a frame-by-frame

basis to ensure alignment with the background/informational video frames. The compositor 406 combines the IPG graphic with the background/informational frames produced by the compositor unit 200 in FIG. 2. The position and size of the IPG graphic with respect to the background is controlled, via the control signal coupled to the compositor 406, by the controller 114 of FIG. 1.

Each of the IPG graphics, e.g., fifteen, are separately composited in this manner with the background and the advertising. As such, fifteen separate bitstreams, one contains each IPG graphic, are encoded and arranged in the transport stream.

FIG. 5A depicts a first illustrative IPG page layout 500_1 as decoded by the decoder of the subscriber equipment. The page 500_1 is one of the fifteen available screens (collectively referred to as IPG pages 500) that can be decoded by appropriate selection of a screen PID within a transport stream. Similar IPG screens can be also decoded from other transport streams that are broadcast to the subscriber equipment from the head end equipment. As decoded, the informational video in regions 504, 506 and 508 plays as any decoded video streams. The audio signal associated with one of the informational video sequences also is decoded and plays in conjunction with the video (i.e., audio follows video). The first IPG graphic 510 contains, for example, program information concerning channels 1 through 10. The subscriber, by manipulating an input device, can scroll through the program selections. As the scrolling function transitions from one cell to another, the cell is highlighted by a change in the on-screen display graphics. These graphics are sent to the subscriber equipment as "user data" and/or "private data" within the transport stream. A detailed description of the operation of the IPG 500 is presented in commonly assigned US patent application _____, filed simultaneously herewith (Attorney docket number 070 CIP2) and herein incorporated by reference.

When the subscriber reaches the bottom of the IPG graphic, i.e., the last cell or a special icon (arrow), a different PID is selected for decoding, i.e., the PID for the next IPG page containing channels 11 through 20. The decoder begins decoding the next stream as soon as it is selected. The connection between IPG pages is a functional attribute that is generally transmitted to the subscriber equipment as user data within the transport stream. Since the background and the informational video were synchronously added to the video sequence that become the IPG pages, the informational video seamlessly transitions from one screen to another without any visible anomalies. The IPG graphic is the only portion that changes from 510_1 to 510_2. The process of transitioning from one IPG page to another can be accomplished by incrementing or decrementing through the IPG pages. Additionally, parallel pages may be available to display additional time slots. As such, IPG pages representing programming in other time periods could be accessed by, for example, left and right arrows. These parallel pages may be carried in additional transport streams or in the same transport stream.

A second illustrative IPG page layout 600 is shown in FIG. 6. This IPG page layout is encoded in the exact same manner as the layout 500 of FIGS. 5A-5C. The IPG of FIG. 6 operates in a similar manner to that of IPG layout 500. The layout 600 is divided vertically such that the informational video, e.g., a video barker, appears on the right half of the layout and the guide region appears on the left. The guide graphics, graphical icons, background imagery, and informational video are combined and then encoded in the same manner as discussed above. A detailed description of the IPG 600 is presented in commonly assigned US patent application _____, filed simultaneously herewith (Attorney docket number 070 CIP2) and herein incorporated by reference.

Although the foregoing description illustratively disclosed encoding an IPG page, the invention finds use in encoding any form of mixed graphical and video information

screens. For example, the invention can be used to encode a HTML web page in the graphics region and a related television program in the video region. Alternatively, the informational video can be a television program that is displayed within a program guide while a viewer reviews the schedule information. Selecting the video region would enlarge the video to the entire screen, while selecting a program title in the program guide may initiate a preview video to play in second video window. As such, the invention should be interpreted as encompassing any combination of video and graphics that is encoded as a digital bit stream and broadcast from a head end of an information distribution system.

Although various embodiments which incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

What is claimed is:

1. A method of producing an encoded user interface comprising:

producing a video frame sequence representing an interactive program guide;

encoding said video frame sequence within a head end of an information distribution system.

2. The method of claim 1 wherein said producing step comprises as step of:

combining, in a frame synchronized manner, background imagery with at least one video sequence and at least one graphic containing program guide information to form said video frame sequence.

3. The method of claim 2 wherein said encoding step further comprises the step of:

encoding the composited frame sequence to compress information therein to form a digital bitstream.

4. The method of claim 2 wherein the combining step further comprises:

compositing, frame-by-frame, at least one video sequence onto said background imagery to form a background sequence; and

compositing a plurality of program guide graphics onto said background sequence, where a different program guide graphic is composited onto said background sequence to form a plurality of program guide frame sequences that represent individual program guide pages.

5. The method of claim 4 wherein said encoding step further comprises:

separately encoding each of said program guide frame sequences to form a digital bitstream for each of the program guide frame sequences.

6. The method of claim 5 further comprising the steps of: multiplexing each of the digital bitstreams into a common transport stream.

7. The method of claim 6 wherein fifteen program guide sequences are formed, encoded, and contained in a common transport stream.

8. The method of claim 5 further comprising:
encoding an audio signal associated with one of the video sequences; and
multiplexing the encoded audio signal into the common transport stream.

9. The method of claim 1 wherein the video frame sequence is a television program.

10. The method of claim 1 wherein the video frame sequence is an advertising program.

11. The method of claim 1 wherein the video frame sequence is encoded using slice based encoding.

12. The method of claim 11 wherein slice based encoding encodes different regions in a different manner than the encoding that is performed upon other portions of the video frame sequence.

13. The method of claim 12 wherein each region is assigned a unique program identifier.

14. The method of claim 8 wherein said multiplexing step further comprises the step of:
multiplexing foreground program guide data into said common transport stream.

15. Apparatus for producing an encoded user interface comprising:

a compositor for producing a frame sequence representing an interactive program guide;

an encoder, coupled to said compositor and located within a head end of an information distribution system, for encoding said frame sequences to form a bitstream.

16. The apparatus of claim 15 wherein said compositor produces a plurality of frame sequences and said encoder comprises a plurality of encoders for encoding each frame sequence in said plurality of frame sequences to form a plurality of bitstreams.

17. The apparatus of claim 16 further comprising

a multiplexer for multiplexing said plurality of bitstreams into a transport stream.

18. The apparatus of claim 17 wherein said multiplexer assigns a different identification code to each said bitstream.

19. The apparatus of claim 17 further comprising a program guide graphics generator for producing said program guide graphics and foreground overlay graphics, where said foreground overlay graphics are included into the transport stream as user data.

20. The apparatus of claim 17 further comprising a program guide graphics generator for producing said program guide graphics and foreground overlay graphics, where said foreground overlay graphics are included into the transport stream as private data.

21. The apparatus of claim 15 wherein said encoder is an MPEG-2 encoder.

22. A bitstream comprising:

a compressed video signal representing one or more program guide pages.

23. The bitstream of claim 22 wherein said compressed video signal is produced using an MPEG encoder.

24. The bitstream of claim 22 wherein said compressed video signal forms a portion of a transport stream.

25. The bitstream of claim 24 wherein said compressed video signal is arranged in packets of data.

26. The bitstream of claim 25 further comprising null packets of data.

27. A method of encoding a plurality of program guide pages comprising the steps of:

encoding each program guide page to form a bitstream representing each program guide page;

determining a longest bitstream;

adding null packets to all bitstreams that are not the longest bitstream until all the bitstreams have the same length; and

adding switching packets to each bitstream.

28. A method of encoding a plurality of program guide pages comprising the steps of:

encoding each program guide page to form a bitstream representing each program guide page;

buffering all the bitstreams for all the guide pages;

retrieving said bitstreams from a buffer;

ordering the bitstreams into a transport stream to equate the length of the transport stream with the length of other transport streams; and

adding switching packets to the transport stream.

29. A method of encoding a plurality of program guide pages comprising the steps of:

encoding each program guide page to form a bitstream representing each program guide page, where said encoding is started at the same time for each program guide page;

assembling a transport stream containing each bitstream in successive order;

adding switching packets into the transport stream after the bitstreams.

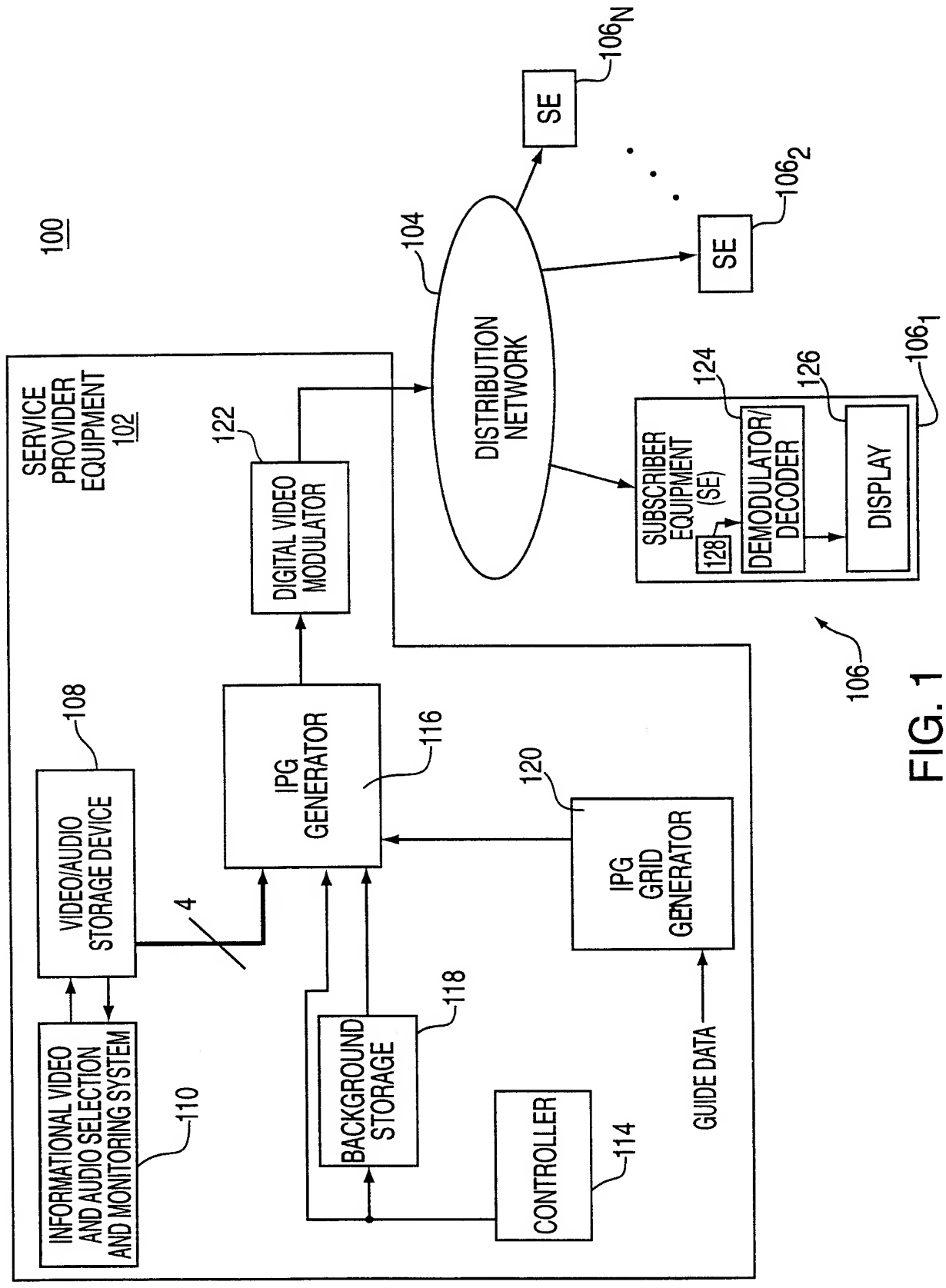
100
SERVICE PROVIDER EQUIPMENT 102
DISTRIBUTION NETWORK
104
SE
106_N
SE
106_2
SUBSCRIBER EQUIPMENT (SE)
128
DEMODULATOR/ DECODER
124
126
DISPLAY
106_1
106
DIGITAL VIDEO MODULATOR
122
IPG GENERATOR
116
VIDEO/AUDIO STORAGE DEVICE
108
4
IPG GRID GENERATOR
120
INFORMATIONAL VIDEO AND AUDIO SELECTION AND MONITORING SYSTEM
110
BACKGROUND STORAGE
118
CONTROLLER
114
GUIDE DATA

FIG. 1

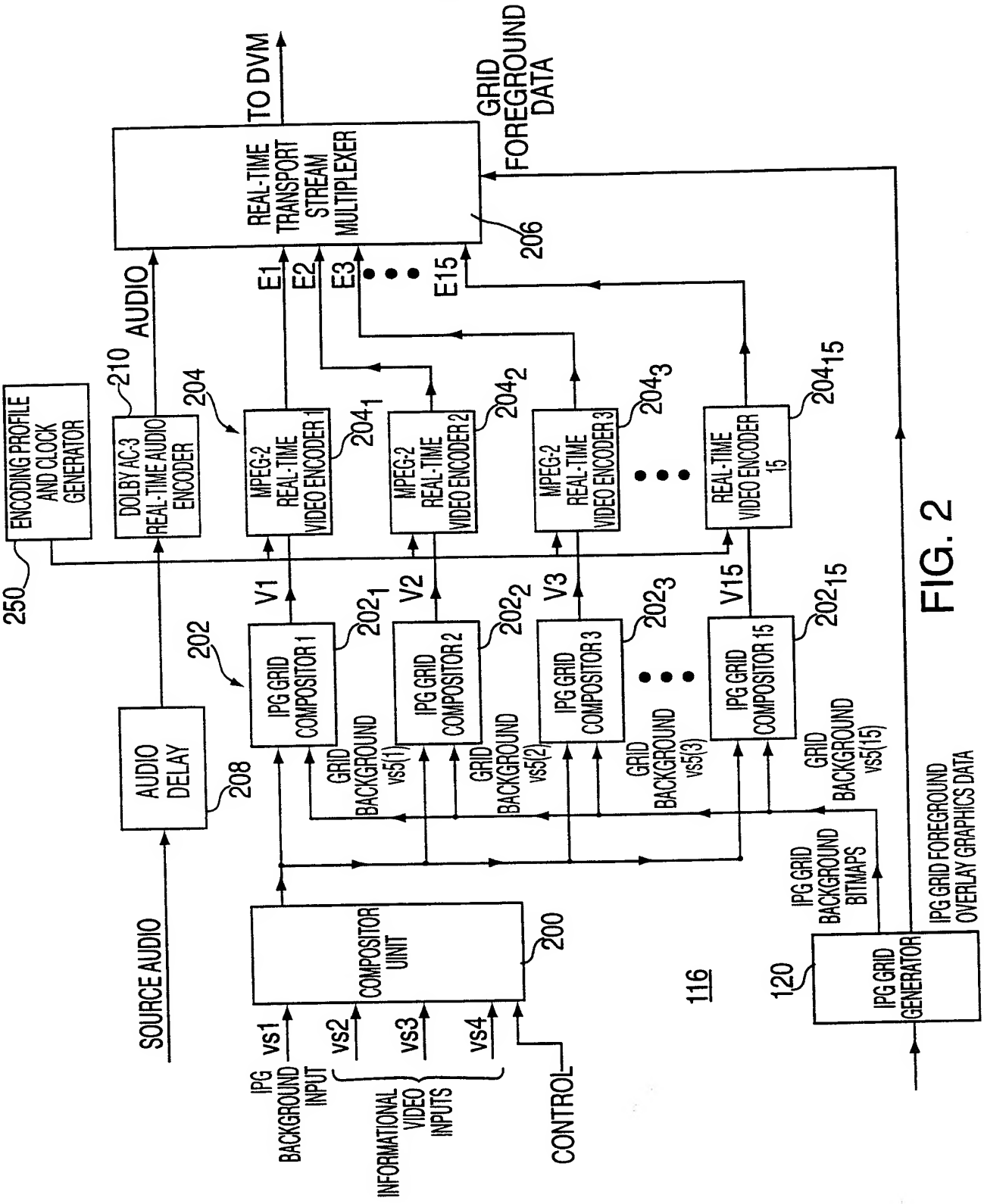
TO DVM
GRID FOREGROUND DATA
REAL-TIME TRANSPORT STREAM MULTIPLEXER
206
E1
E2
E3
E15
AUDIO
210
ENCODING PROFILE AND CLOCK GENERATOR
DOLBY AC-3 REAL-TIME AUDIO ENCODER
204
MPEG-2 REAL-TIME VIDEO ENCODER 1
204_1
MPEG-2 REAL-TIME VIDEO ENCODER 2
204_2
MPEG-2 REAL-TIME VIDEO ENCODER 3
204_3
REAL-TIME VIDEO ENCODER 15
204_{15}
250
V1
V2
V3
V15
202
IPG GRID COMPOSITOR 1
202_1
IPG GRID COMPOSITOR 2
202_2
IPG GRID COMPOSITOR 3
202_3
IPG GRID COMPOSITOR 15
202_{15}
AUDIO DELAY
208
GRID BACKGROUND vs5(1)
GRID BACKGROUND vs5(2)
GRID BACKGROUND vs5(3)
GRID BACKGROUND vs5(15)
IPG GRID BACKGROUND BITMAPS
IPG GRID FOREGROUND OVERLAY GRAPHICS DATA
SOURCE AUDIO
COMPOSITOR UNIT
200
116
120
IPG GRID GENERATOR
vs1
vs2
vs3
vs4
IPG BACKGROUND INPUT
INFORMATIONAL VIDEO INPUTS
CONTROL

FIG. 2

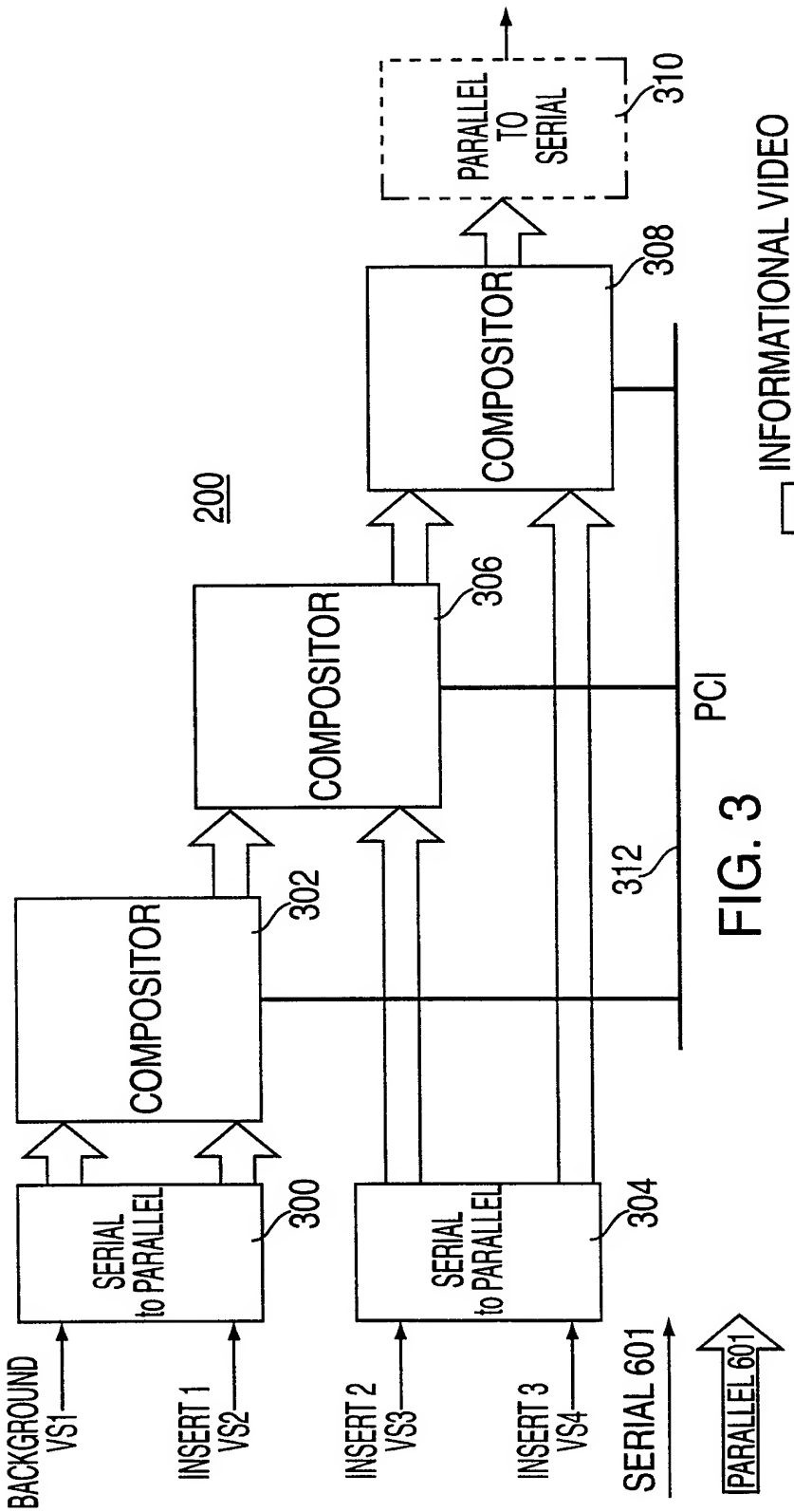
200
BACKGROUND VS1
INSERT 1 VS2
INSERT 2 VS3
INSERT 3 VS4
SERIAL to PARALLEL
300
SERIAL to PARALLEL
304
COMPOSITOR
302
COMPOSITOR
306
COMPOSITOR
308
PARALLEL TO SERIAL
310
312
PCI
SERIAL 601
PARALLEL 601

FIG. 3

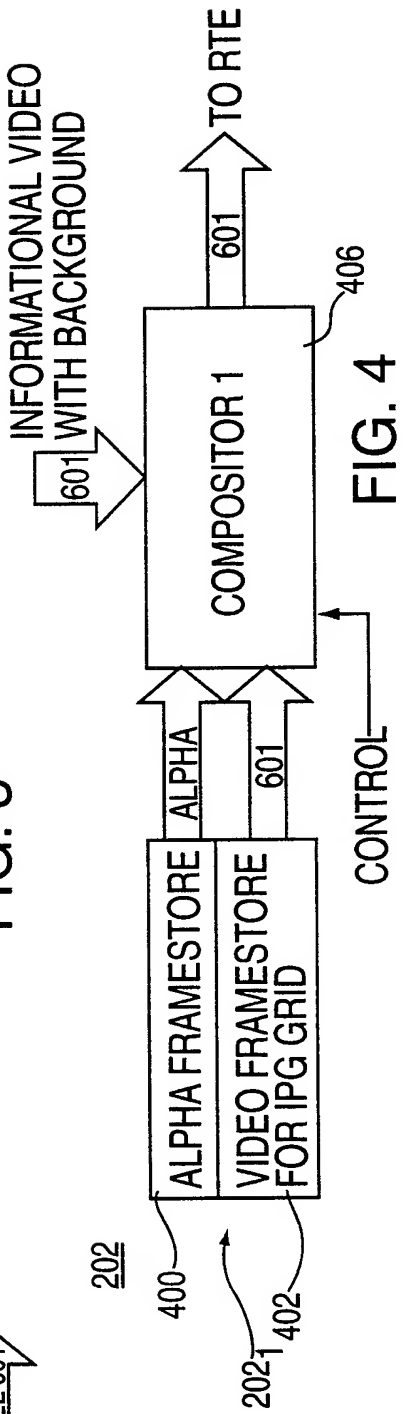
INFORMATIONAL VIDEO WITH BACKGROUND
601
COMPOSITOR 1
406
601
TO RTE
ALPHA
601
CONTROL
ALPHA FRAMESTORE
VIDEO FRAMESTORE FOR IPG GRID
202
400
402
201

FIG. 4

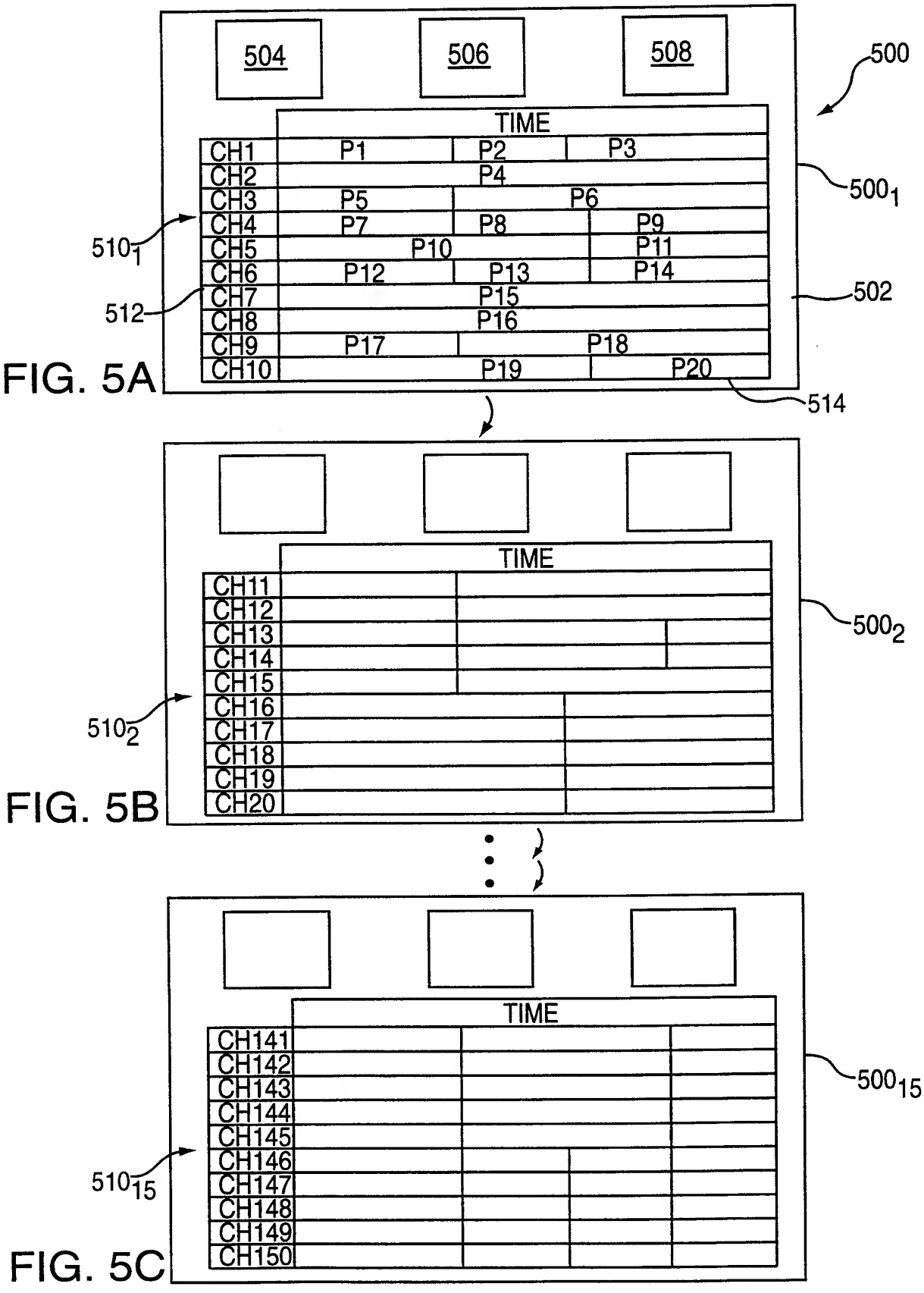

FIG. 5A

FIG. 5B

FIG. 5C

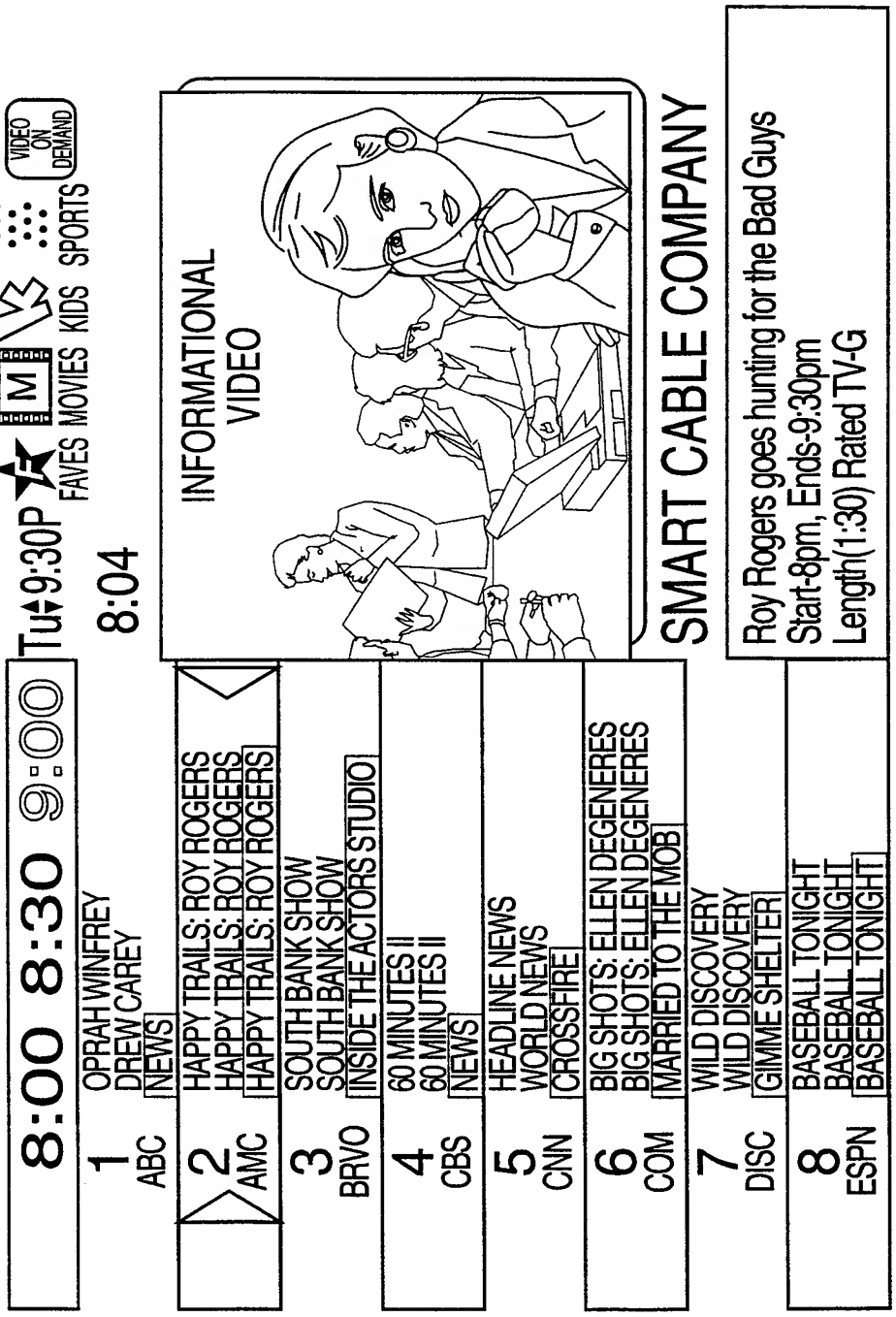
8:00 8:30 9:00
Tu 9:30P
FAVES
MOVIES
KIDS
SPORTS
VIDEO ON DEMAND
8:04
1 ABC OPRAH WINFREY DREW CAREY NEWS
2 AMC HAPPY TRAILS: ROY ROGERS HAPPY TRAILS: ROY ROGERS HAPPY TRAILS: ROY ROGERS
3 BRVO SOUTH BANK SHOW SOUTH BANK SHOW INSIDE THE ACTORS STUDIO
4 CBS 60 MINUTES II 60 MINUTES II NEWS
5 CNN HEADLINE NEWS WORLD NEWS CROSSFIRE
6 COM BIG SHOTS: ELLEN DEGENERES BIG SHOTS: ELLEN DEGENERES MARRIED TO THE MOB
7 DISC WILD DISCOVERY WILD DISCOVERY GIMME SHELTER
8 ESPN BASEBALL TONIGHT BASEBALL TONIGHT BASEBALL TONIGHT
INFORMATIONAL VIDEO
SMART CABLE COMPANY
Roy Rogers goes hunting for the Bad Guys
Start-8pm, Ends-9:30pm
Length(1:30) Rated TV-G
600

FIG. 6

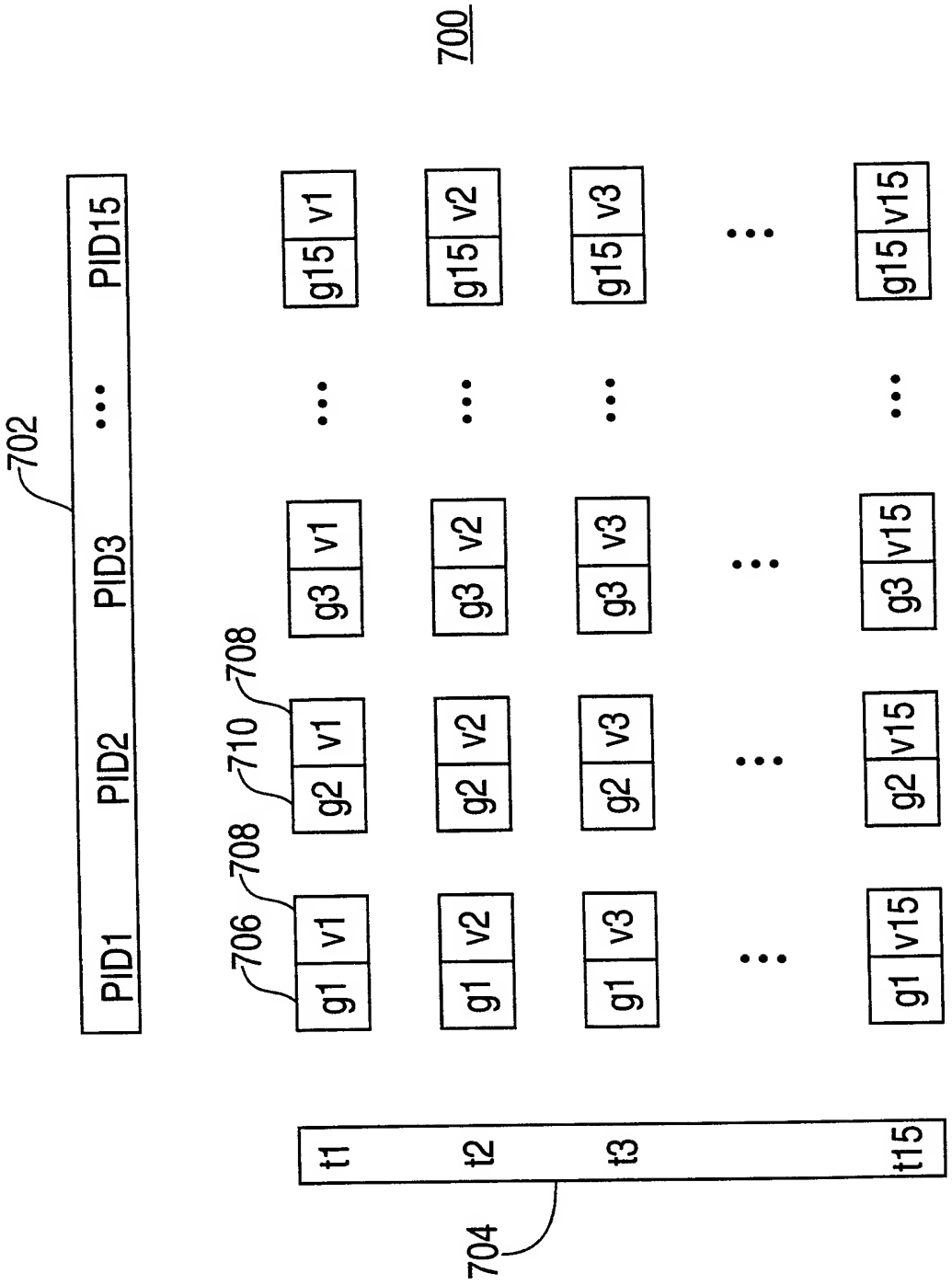
700
702
PID1
PID2
PID3
PID15
706
708
710
g1 v1
g2 v1
g3 v1
g15 v1
g1 v2
g2 v2
g3 v2
g15 v2
g1 v3
g2 v3
g3 v3
g15 v3
g1 v15
g2 v15
g3 v15
g15 v15
t1
t2
t3
t15
704

FIG. 7

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/US 99/16265

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 94 14282 A (DISCOVERY COMMUNICAT INC) 23 June 1994 (1994-06-23) page 15, line 6 -page 18, line 4 page 78, line 16 - line 20 page 82, line 6 -page 83, line 22 figures 20-27 ---	1-25,28, 29
X	EP 0 838 958 A (THOMSON CONSUMER ELECTRONICS) 29 April 1998 (1998-04-29) page 3, column 3, line 50 -page 5, column 8, line 47 figures 1-7 --- -/--	22-29

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 October 1999	18/10/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Van der Zaal, R

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/US 99/16265

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte ional Application No
PCT/US 99/16265

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International Application No
PCT/US 99/16265

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